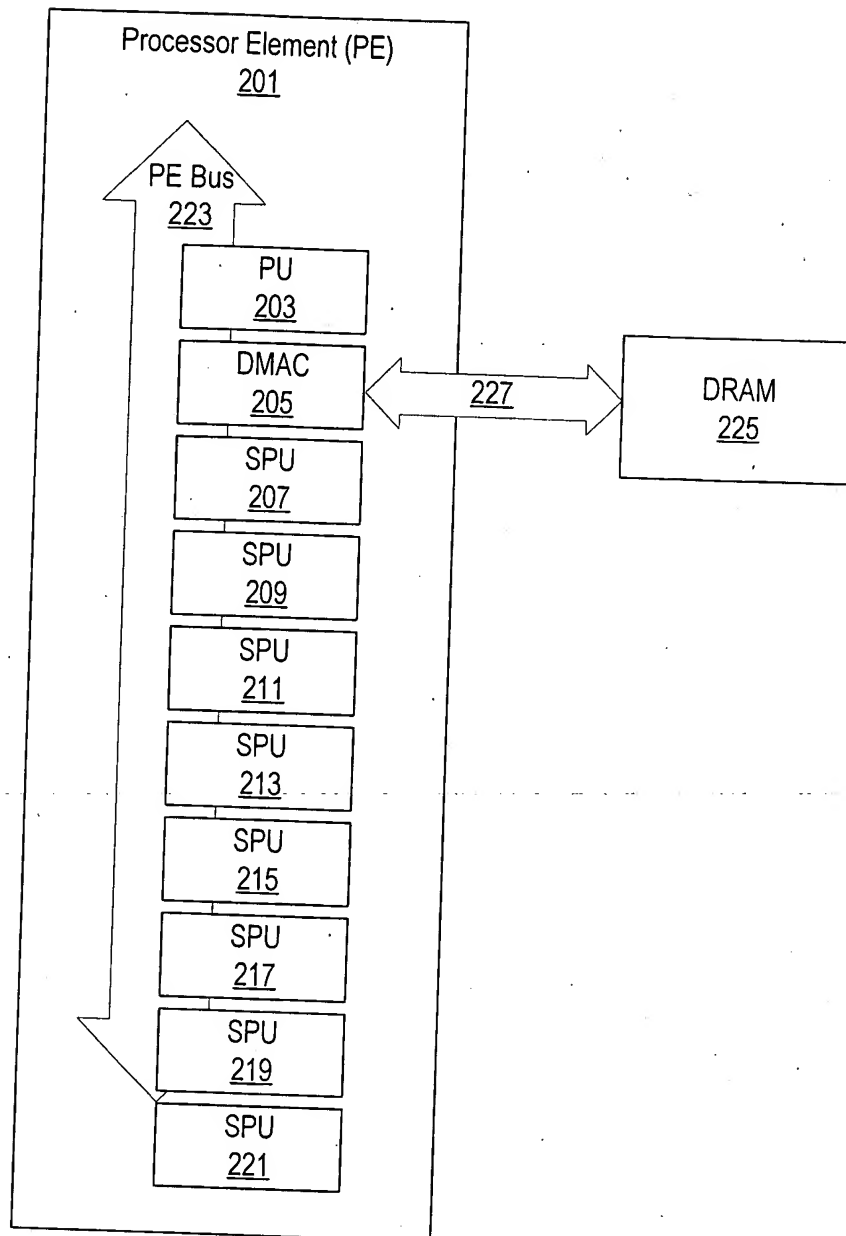
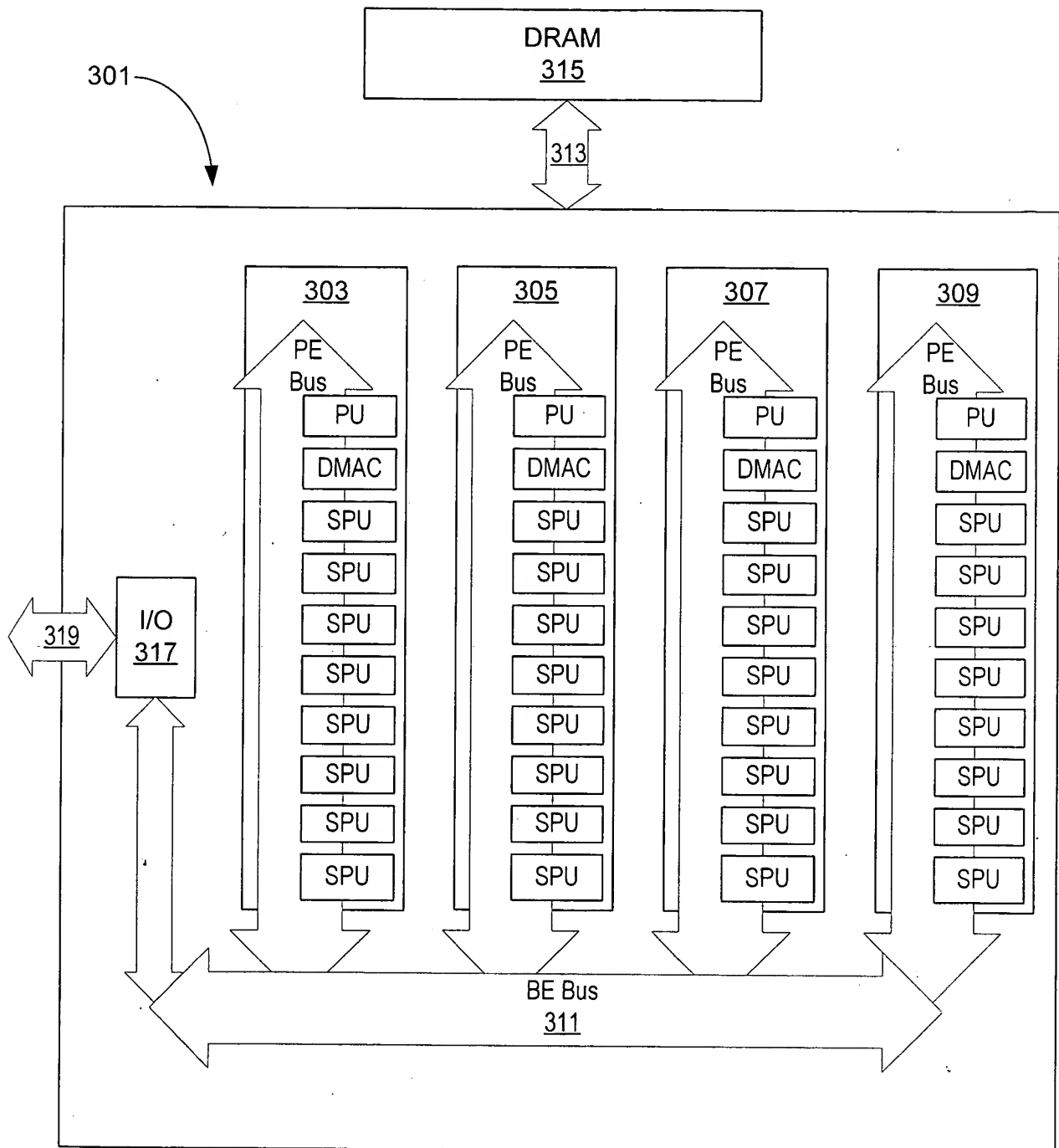


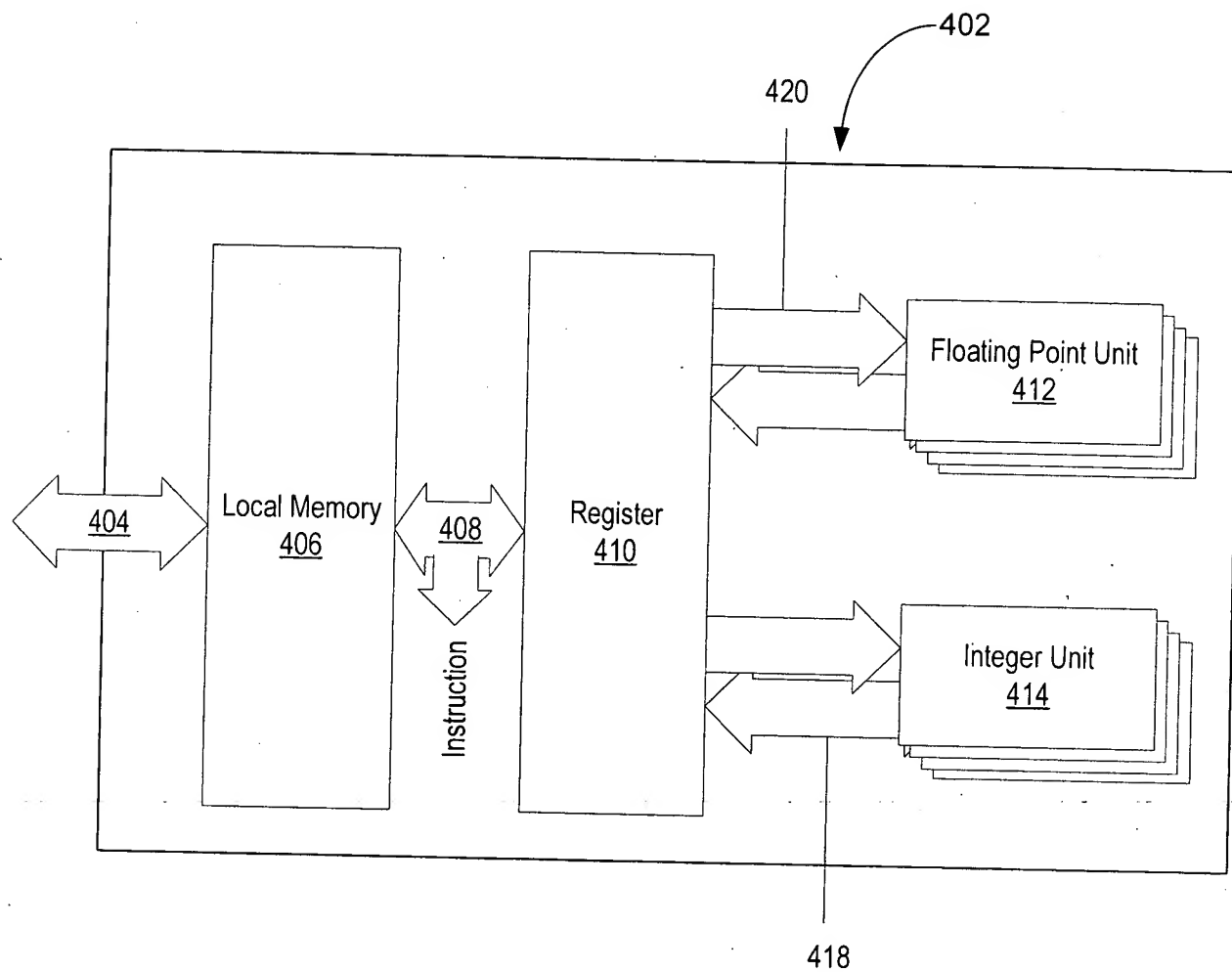
Figure 1

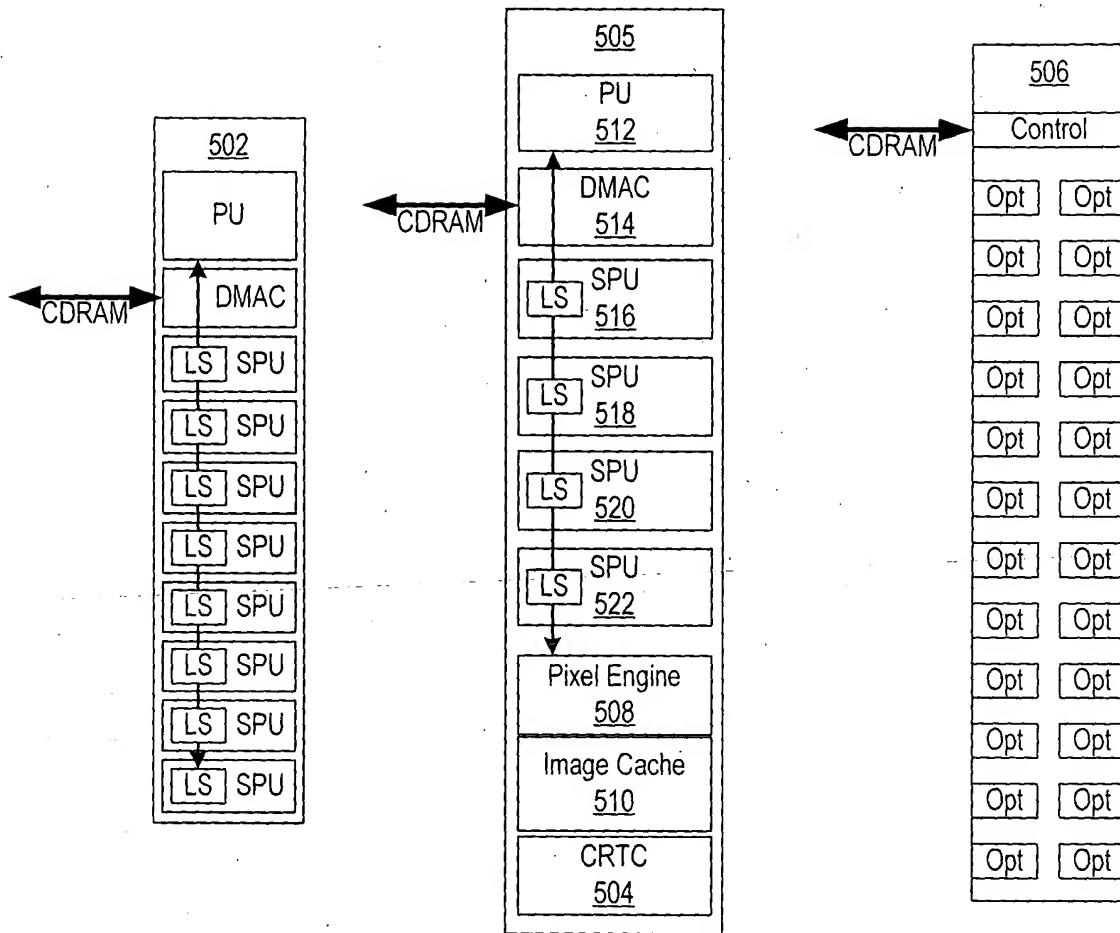
**Figure 2**

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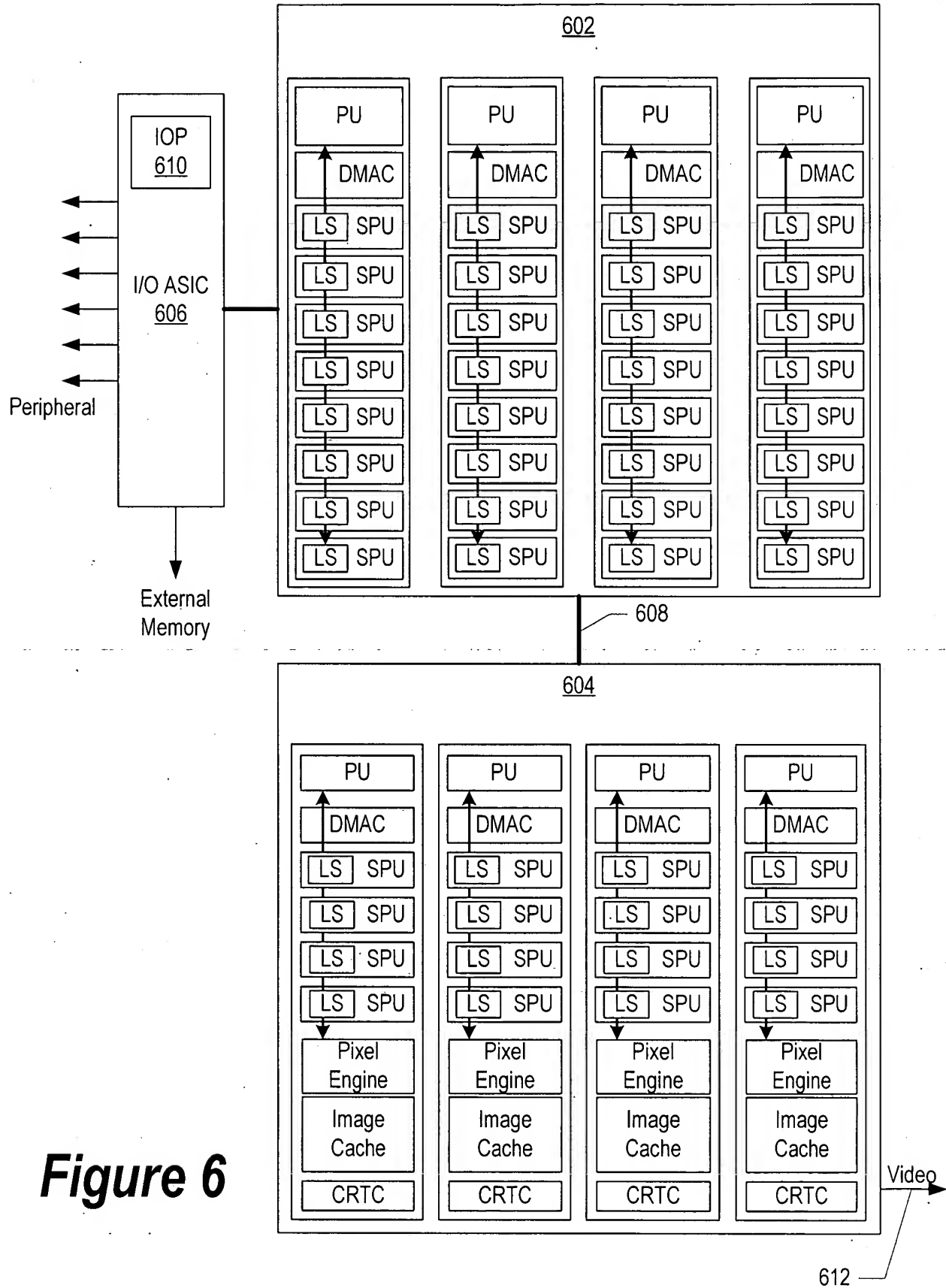
**Figure 3**

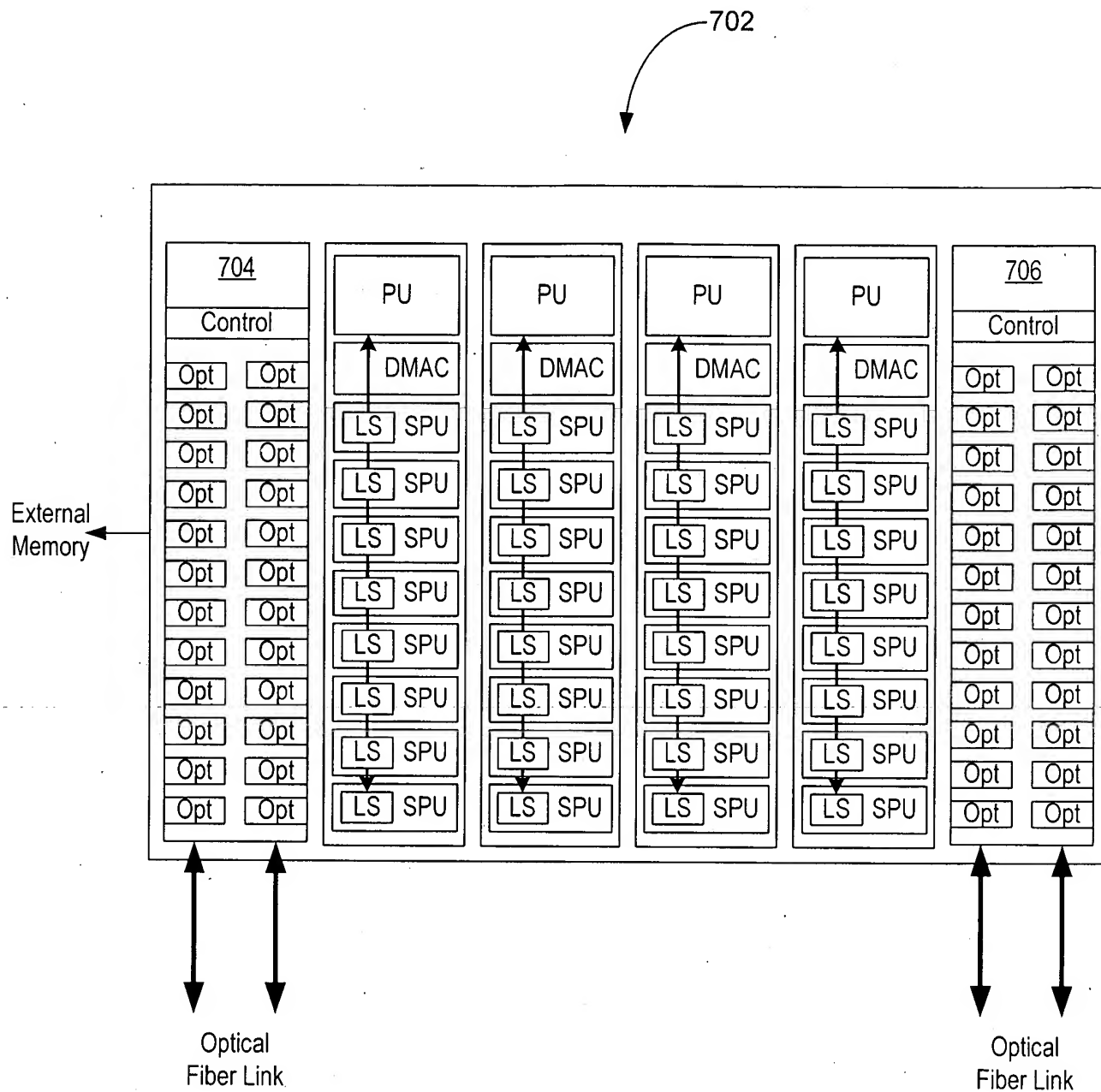
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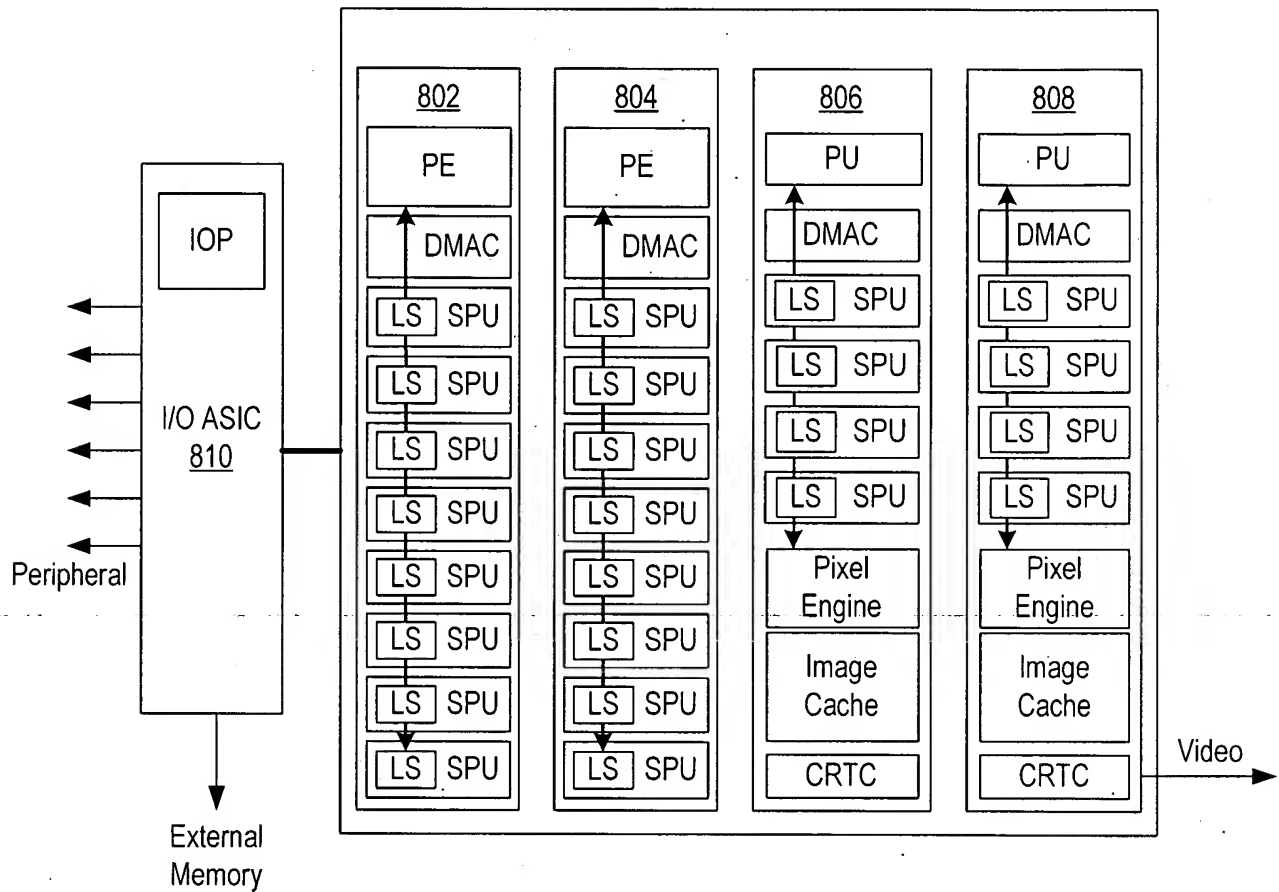
**Figure 4**

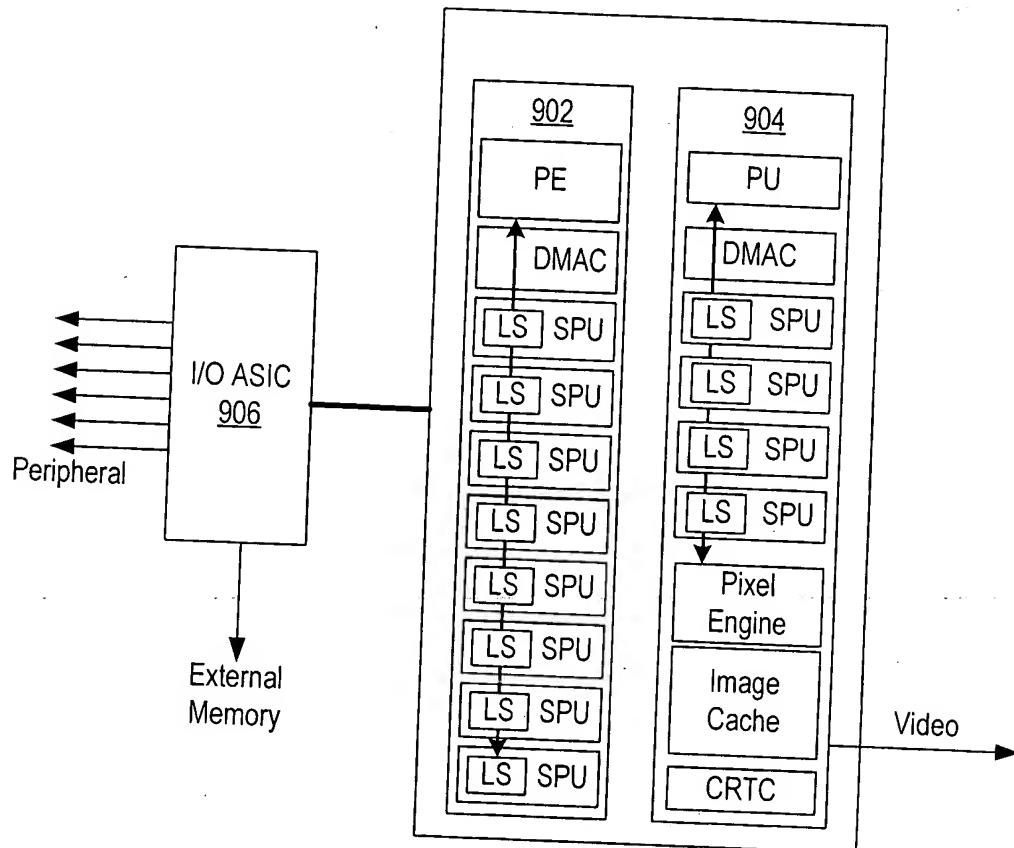
**Figure 5**

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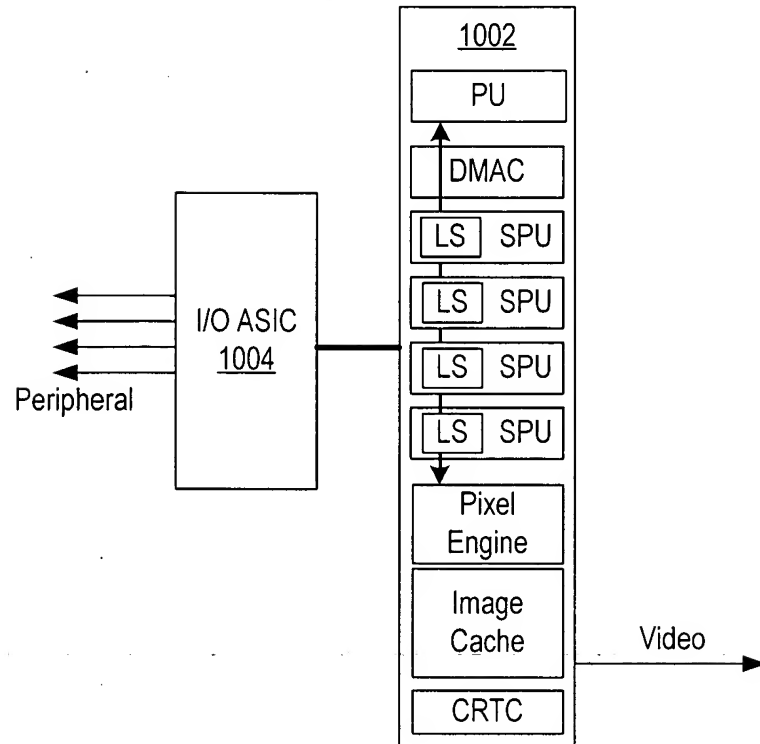
**Figure 6**

**Figure 7**

**Figure 8**

**Figure 9**

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**Figure 10**

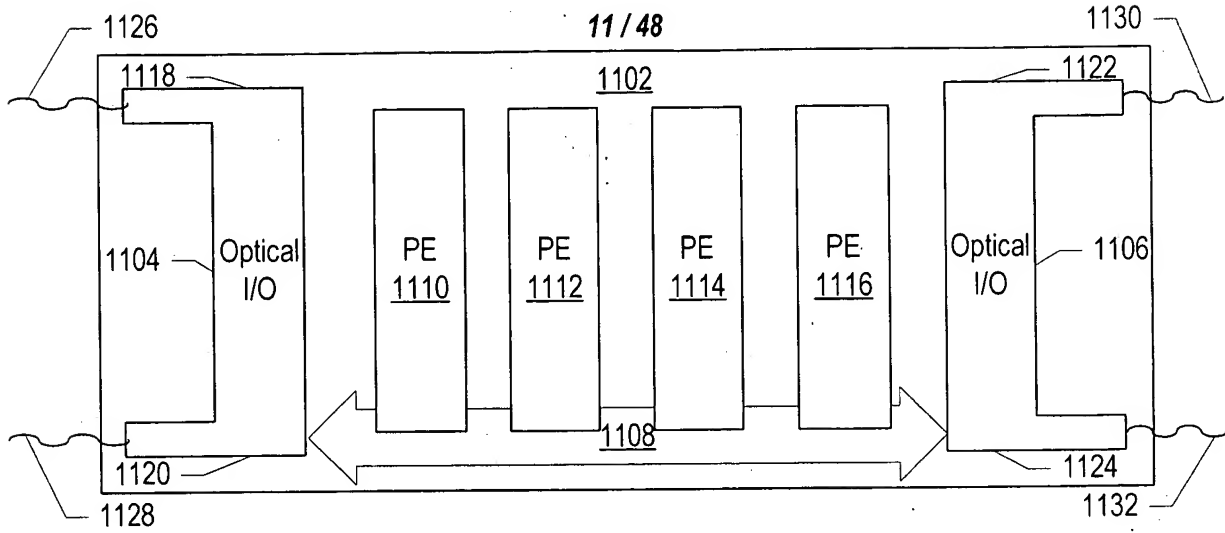


Figure 11A

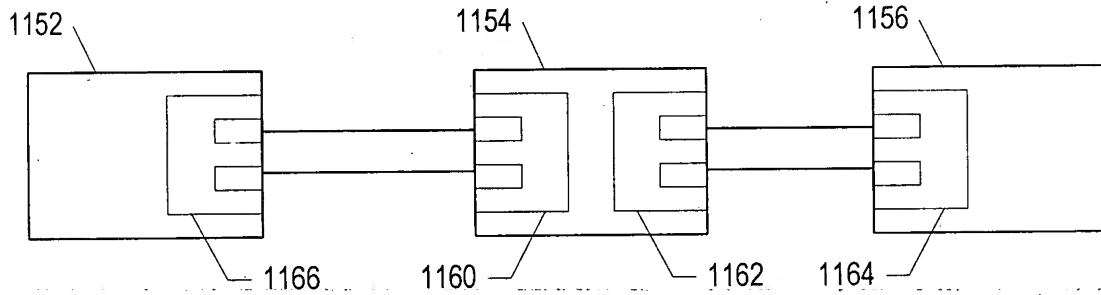


Figure 11B

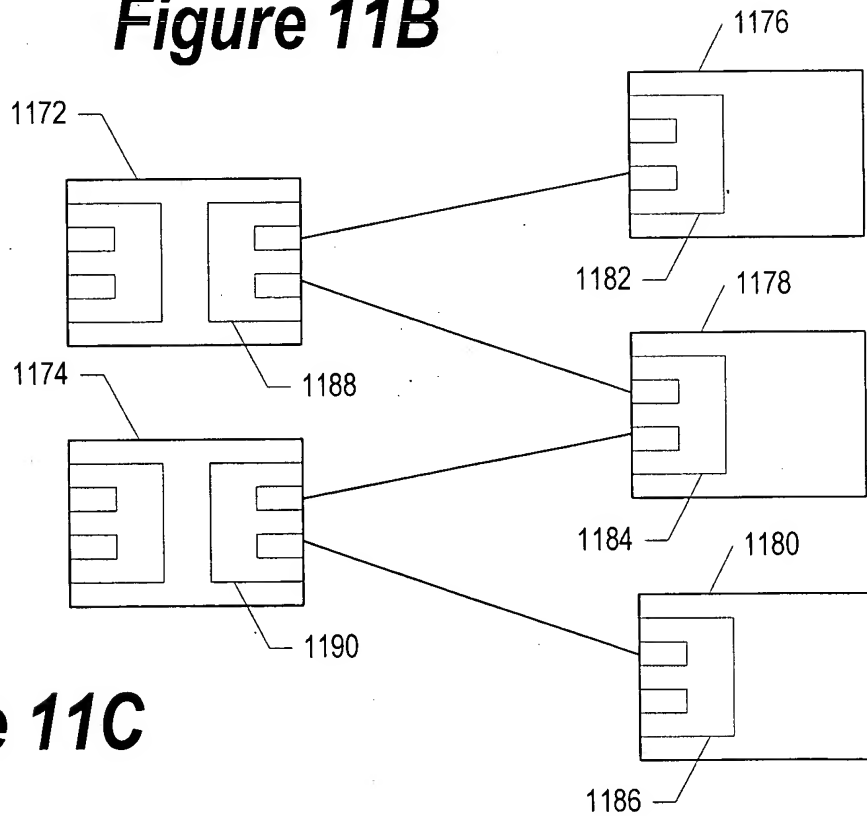
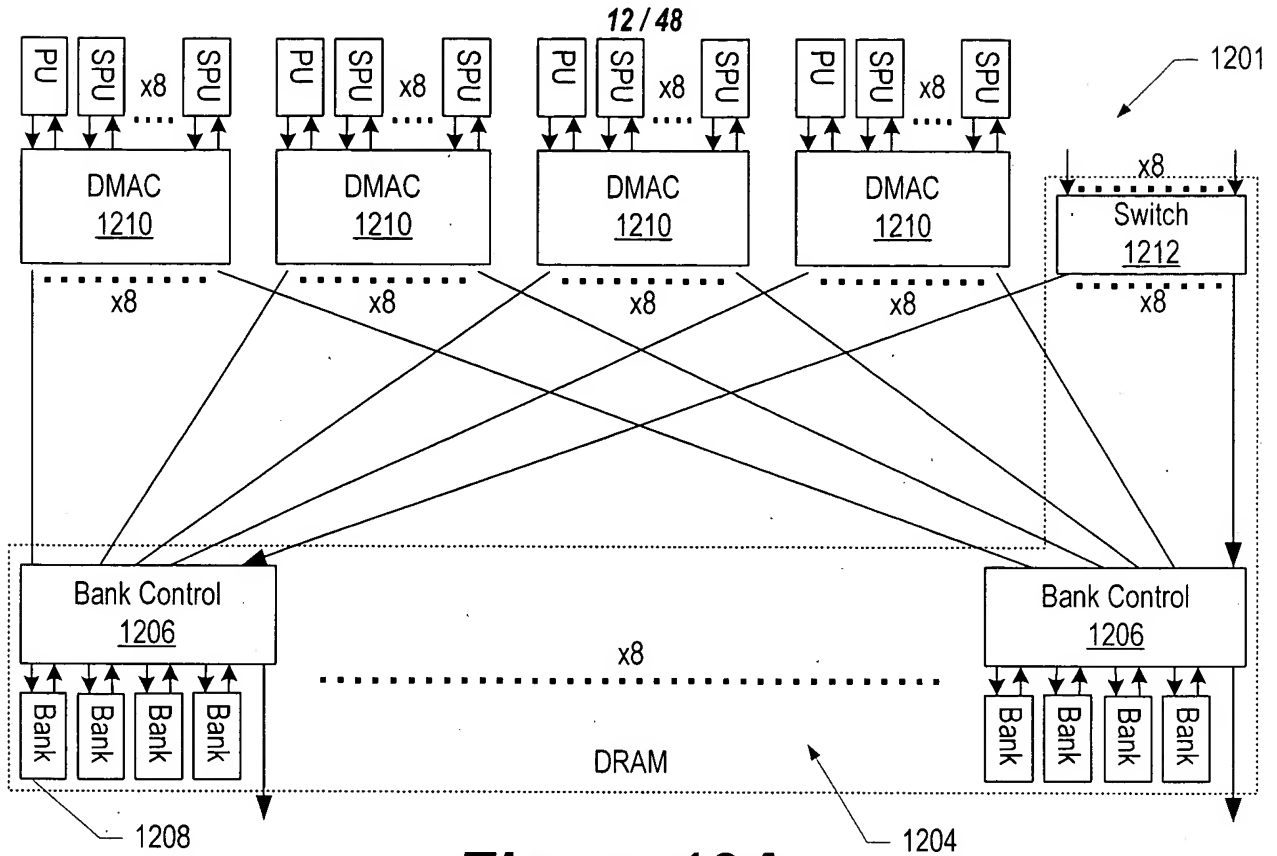
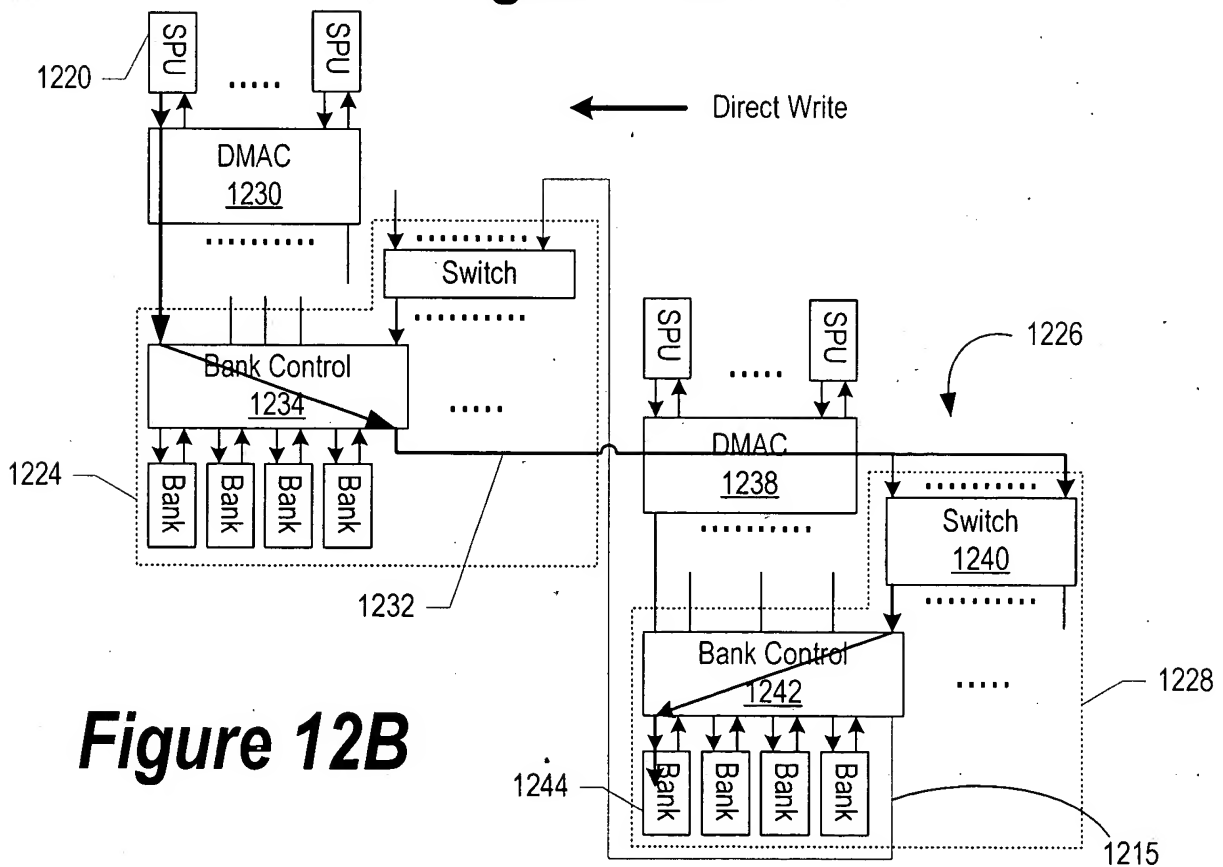


Figure 11C

**Figure 12A****Figure 12B**

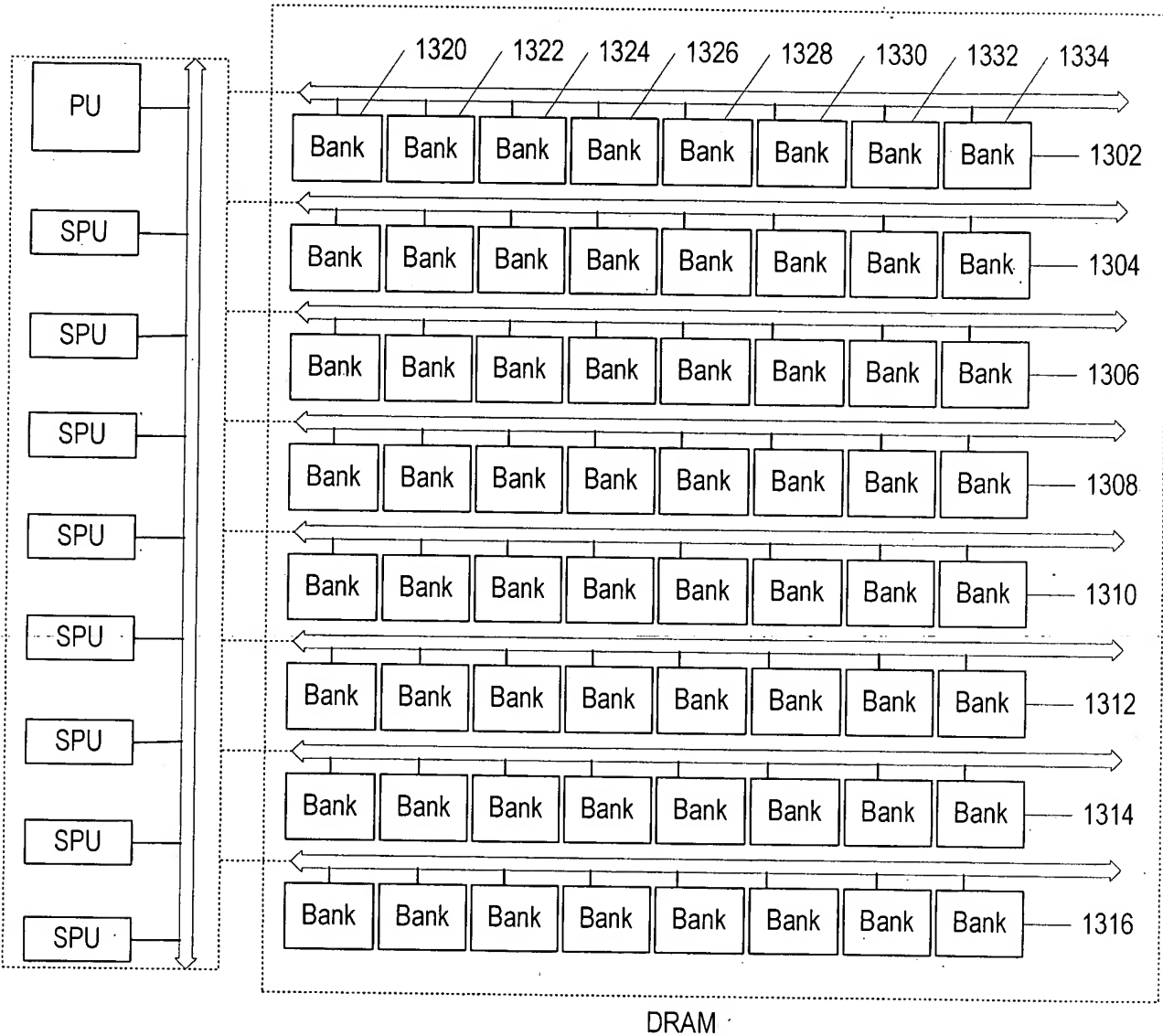


Figure 13

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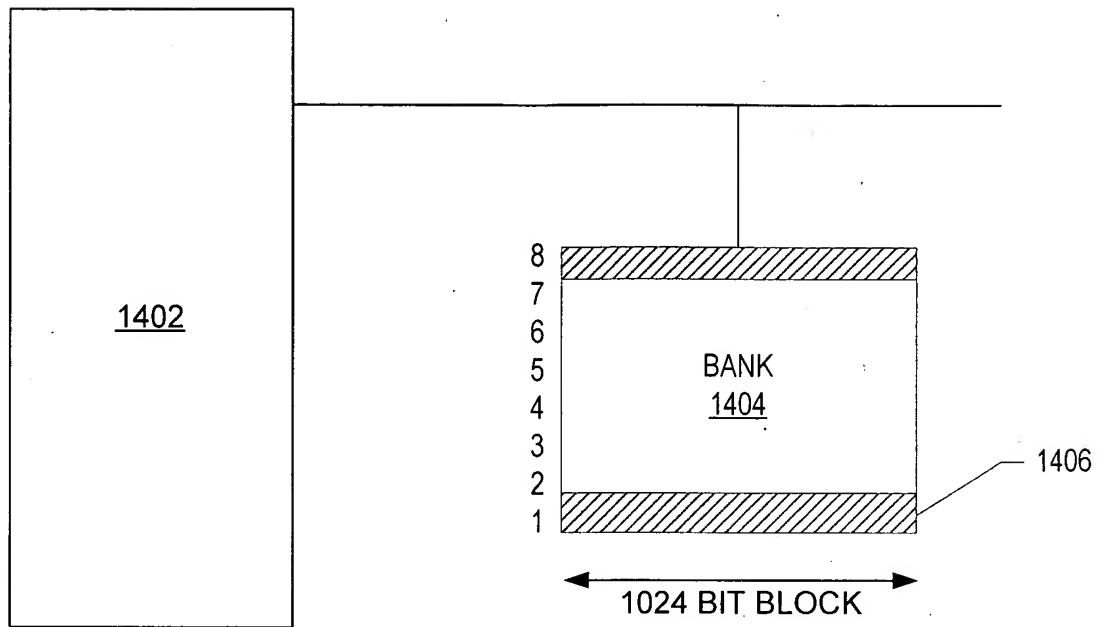


Figure 14A

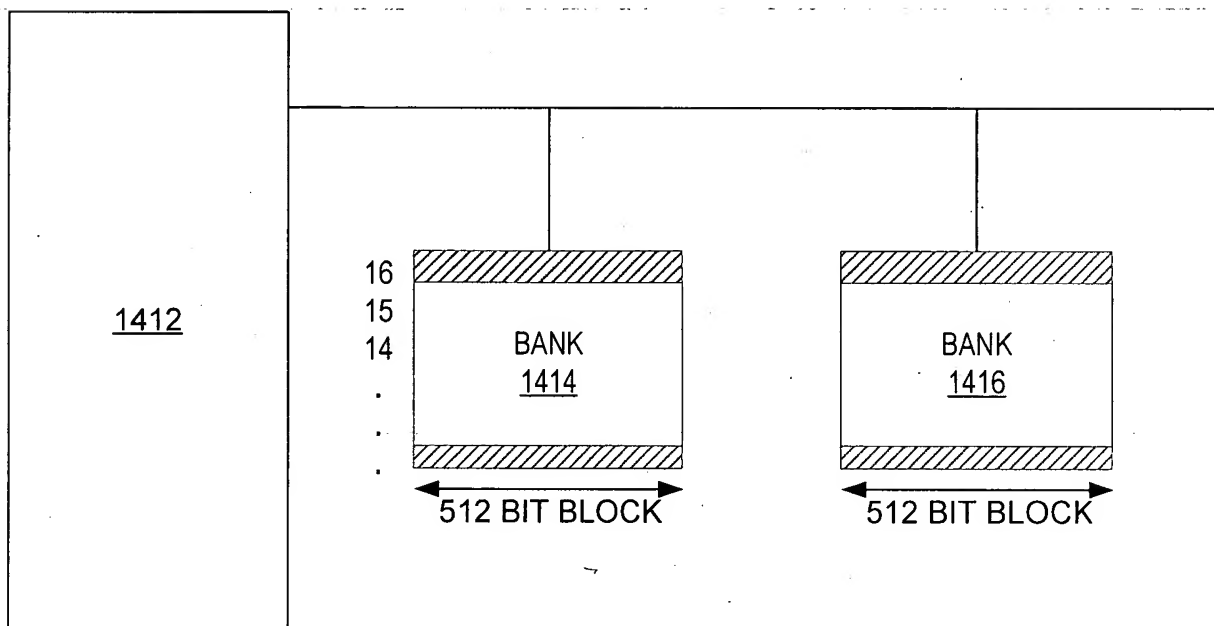


Figure 14B

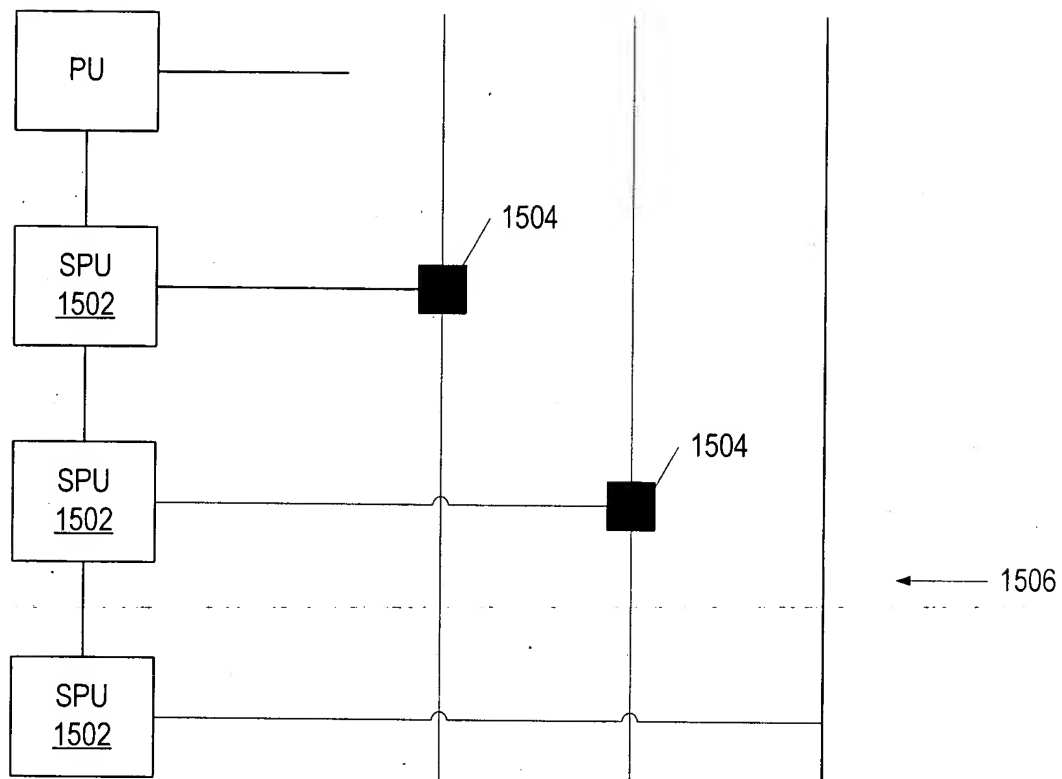


Figure 15

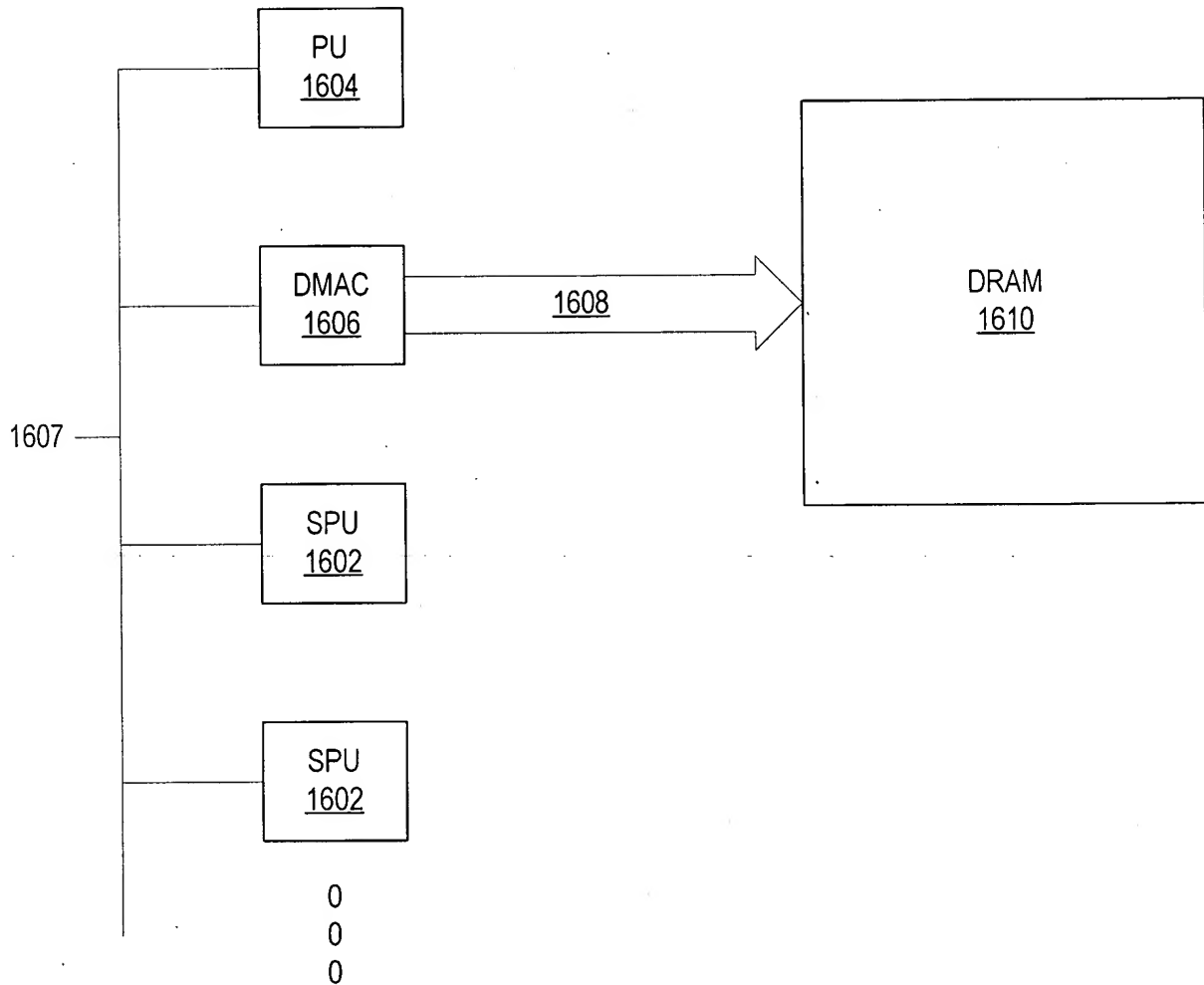
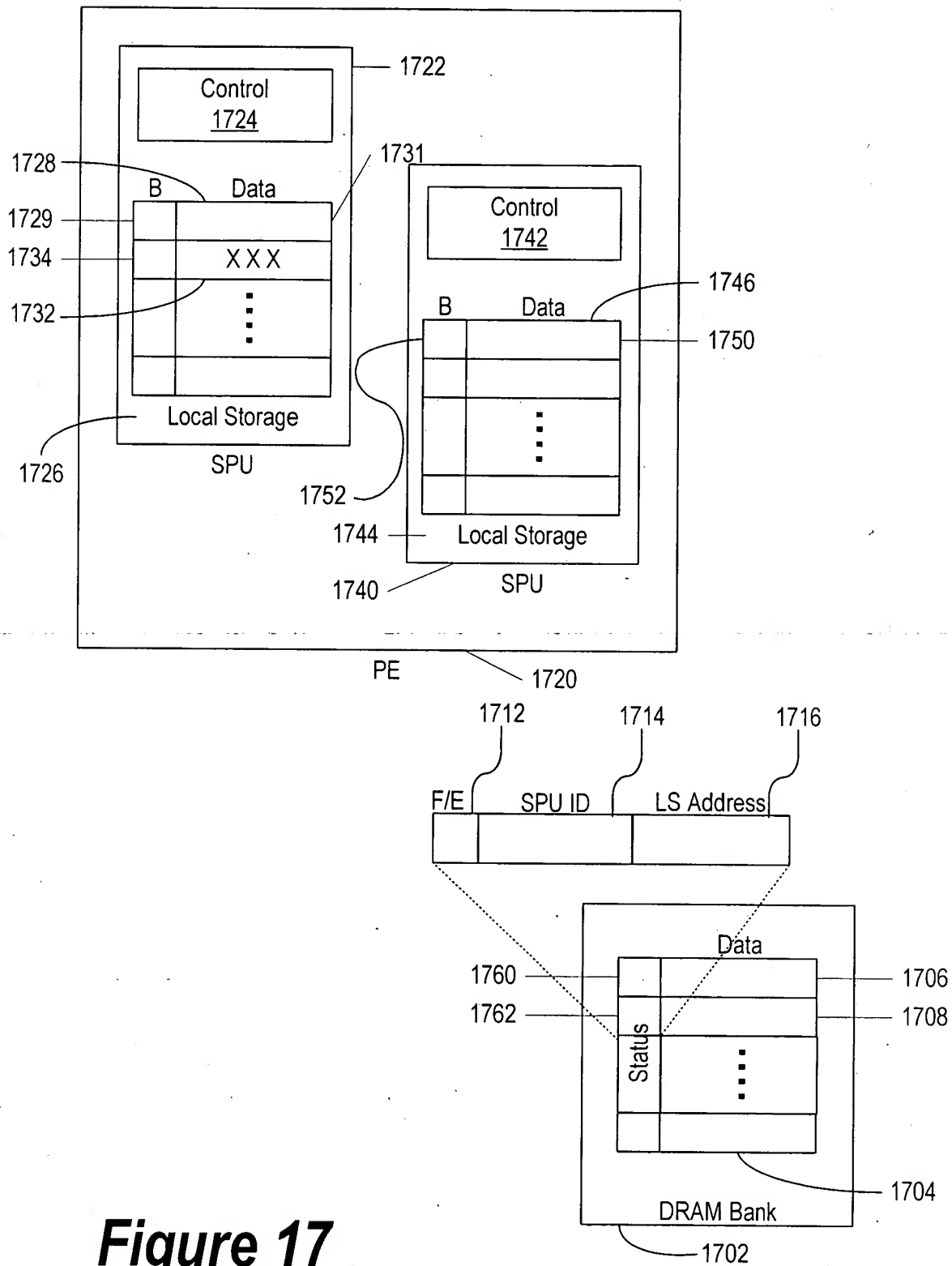


Figure 16

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**Figure 17**

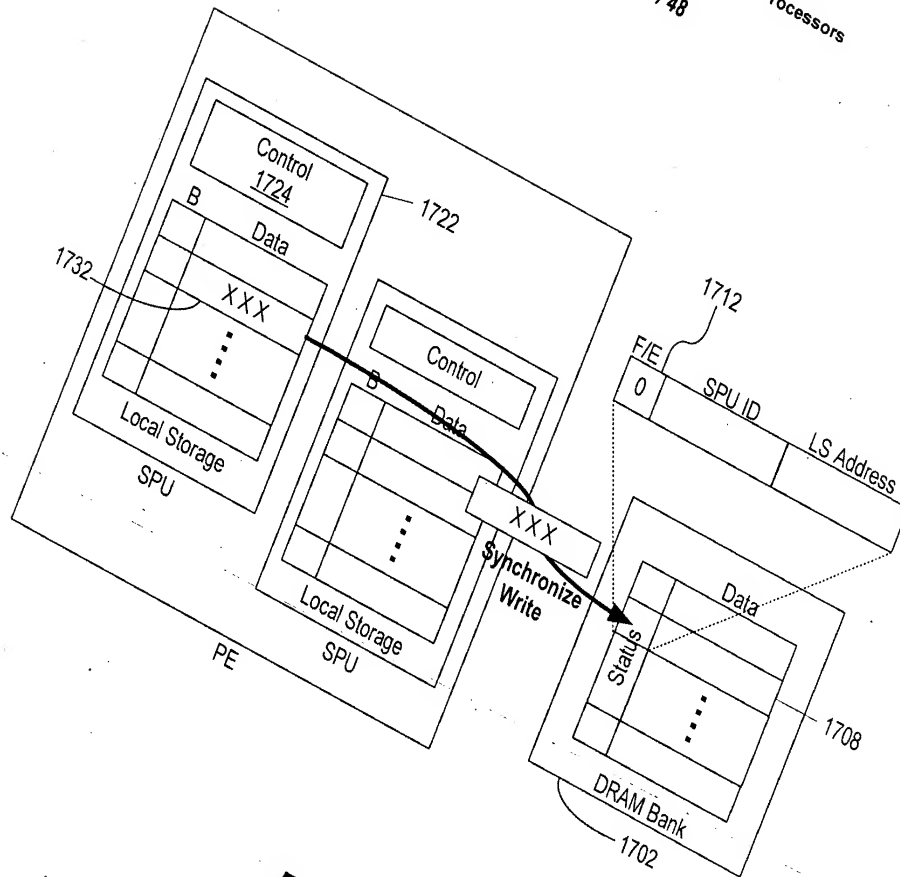


Figure 18

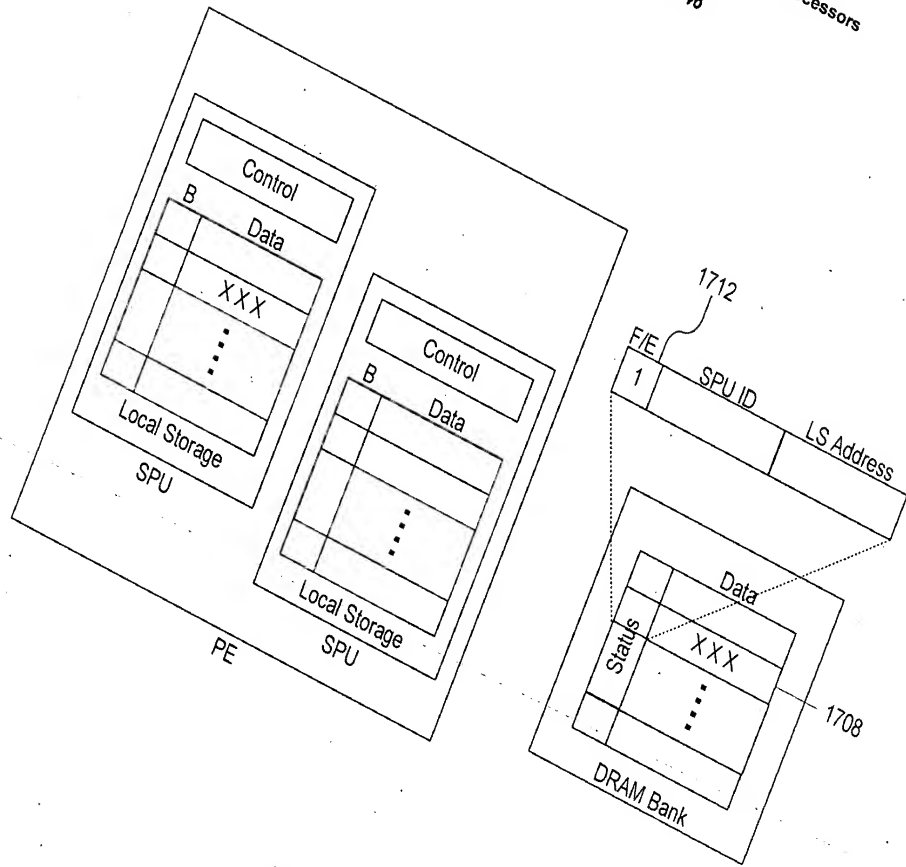
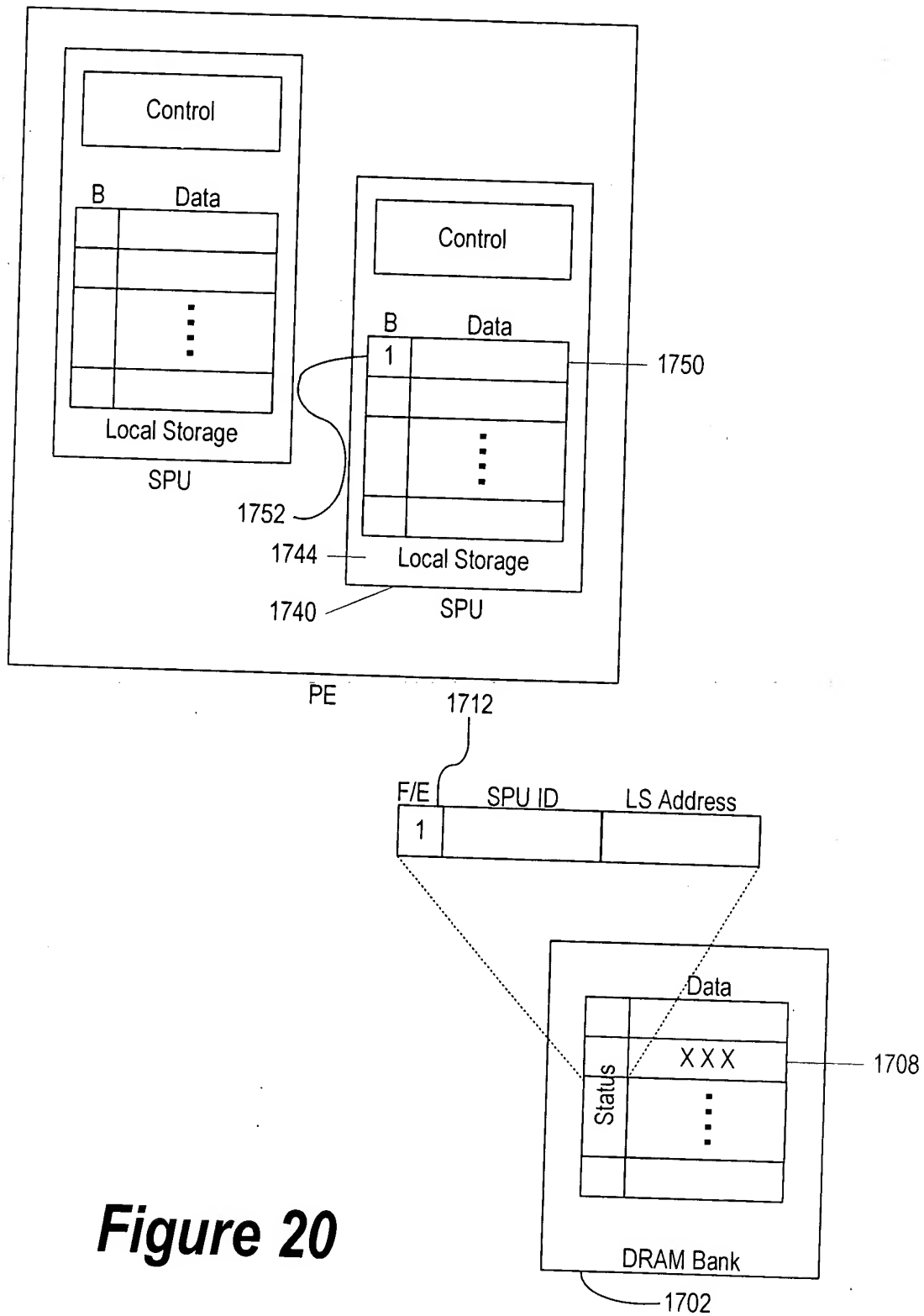


Figure 19

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**Figure 20**

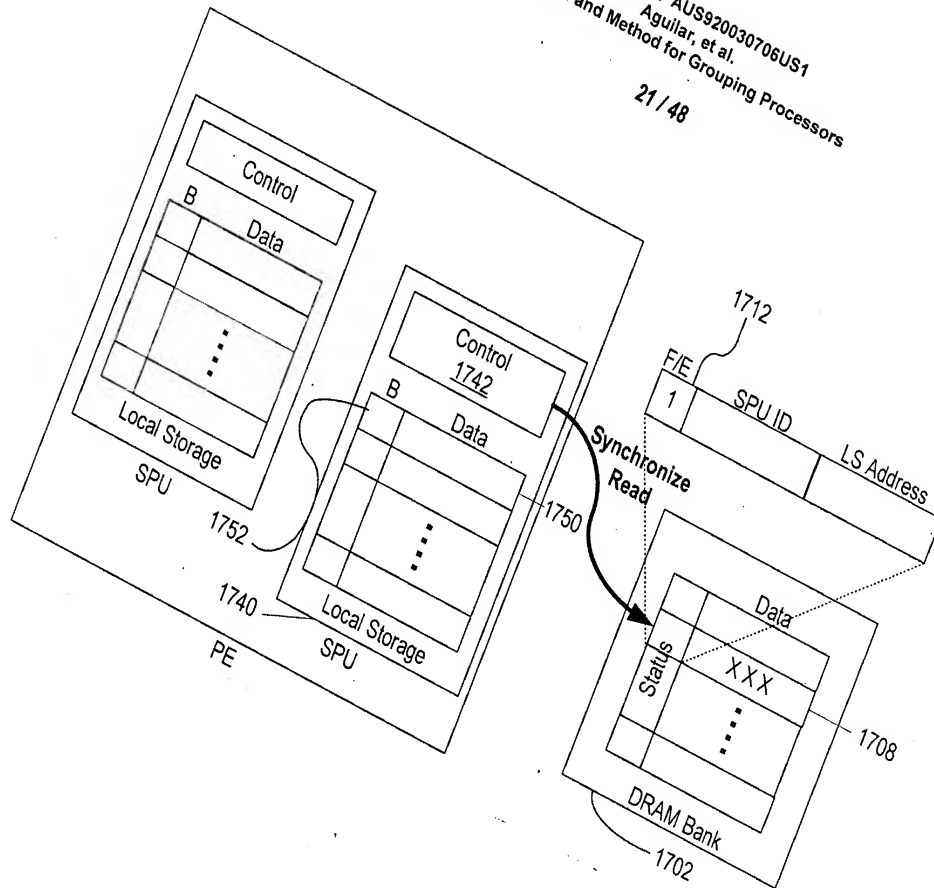
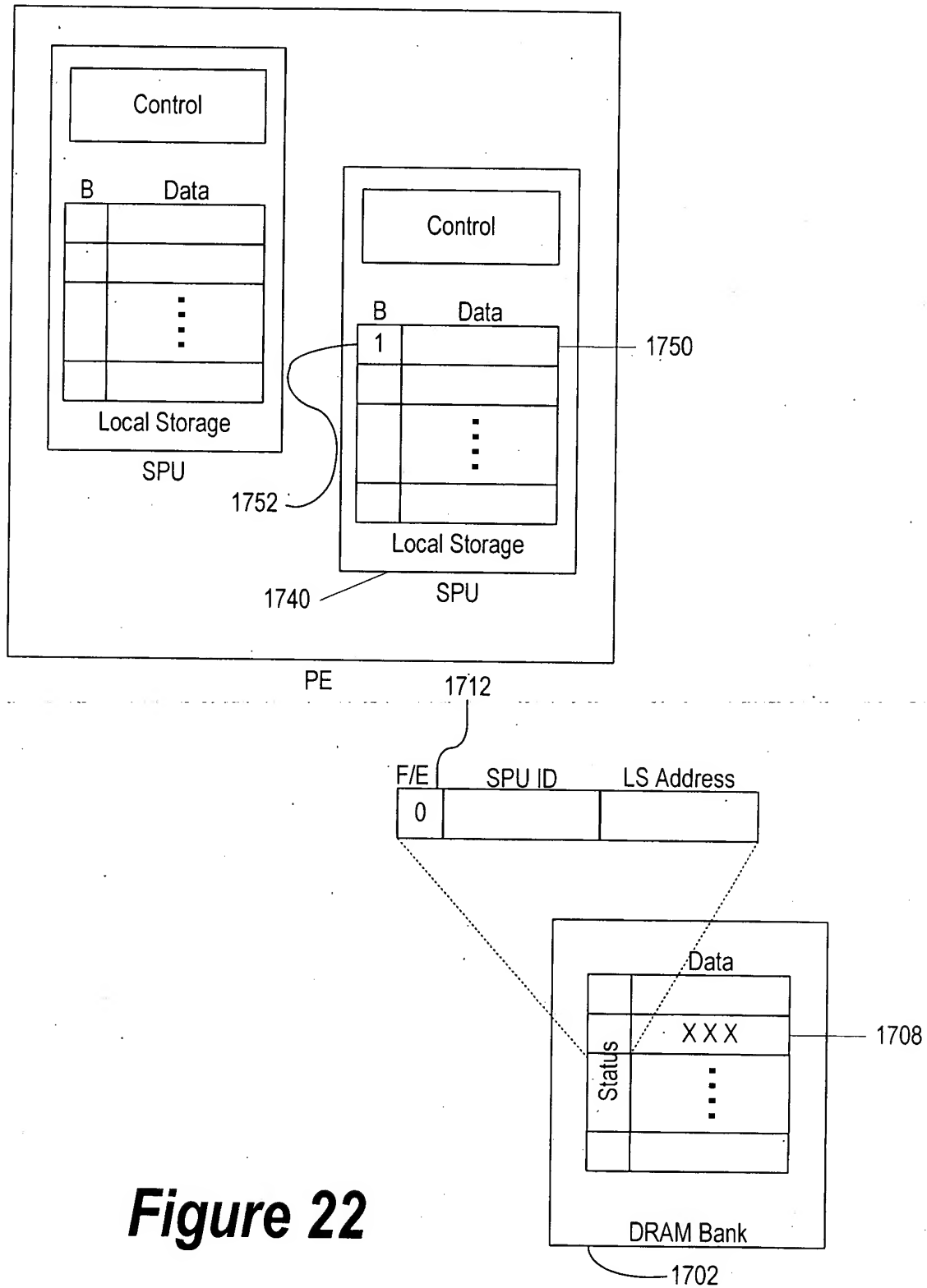


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**Figure 22**

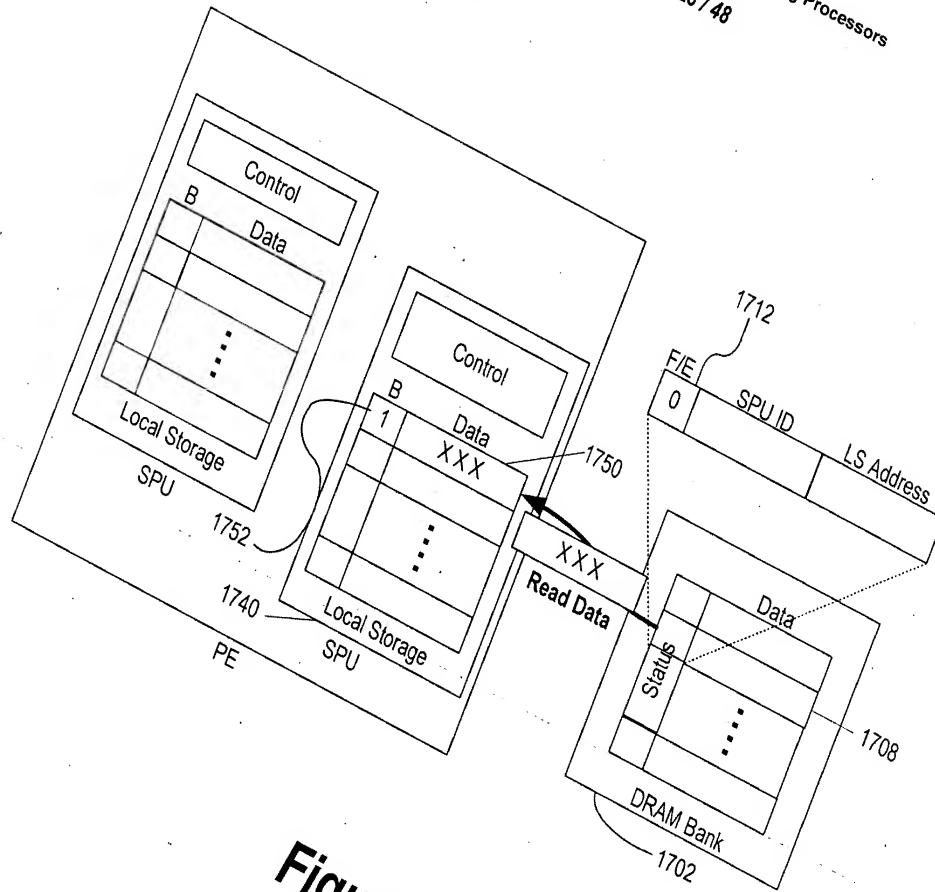
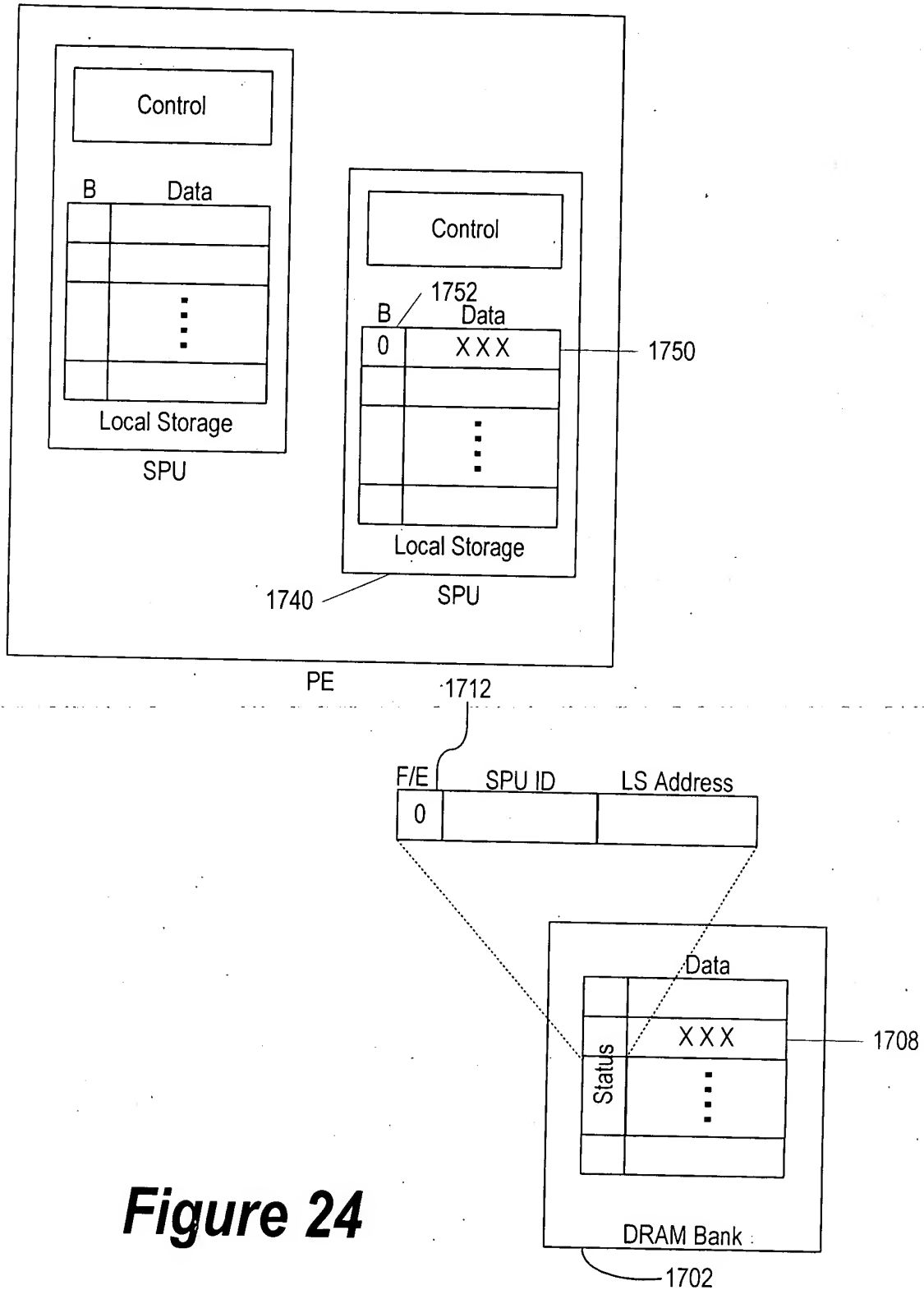
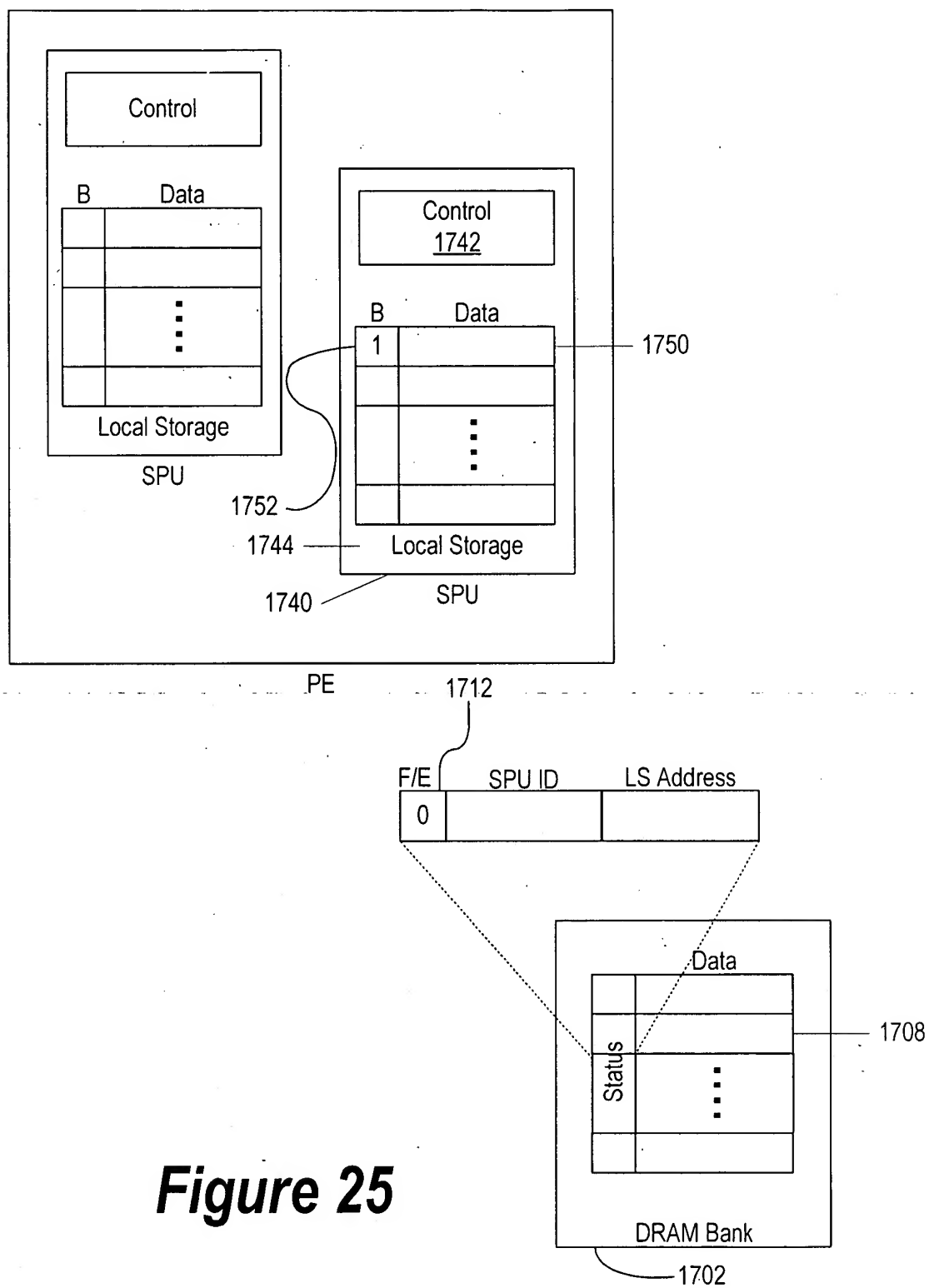


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**Figure 24**

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**Figure 25**

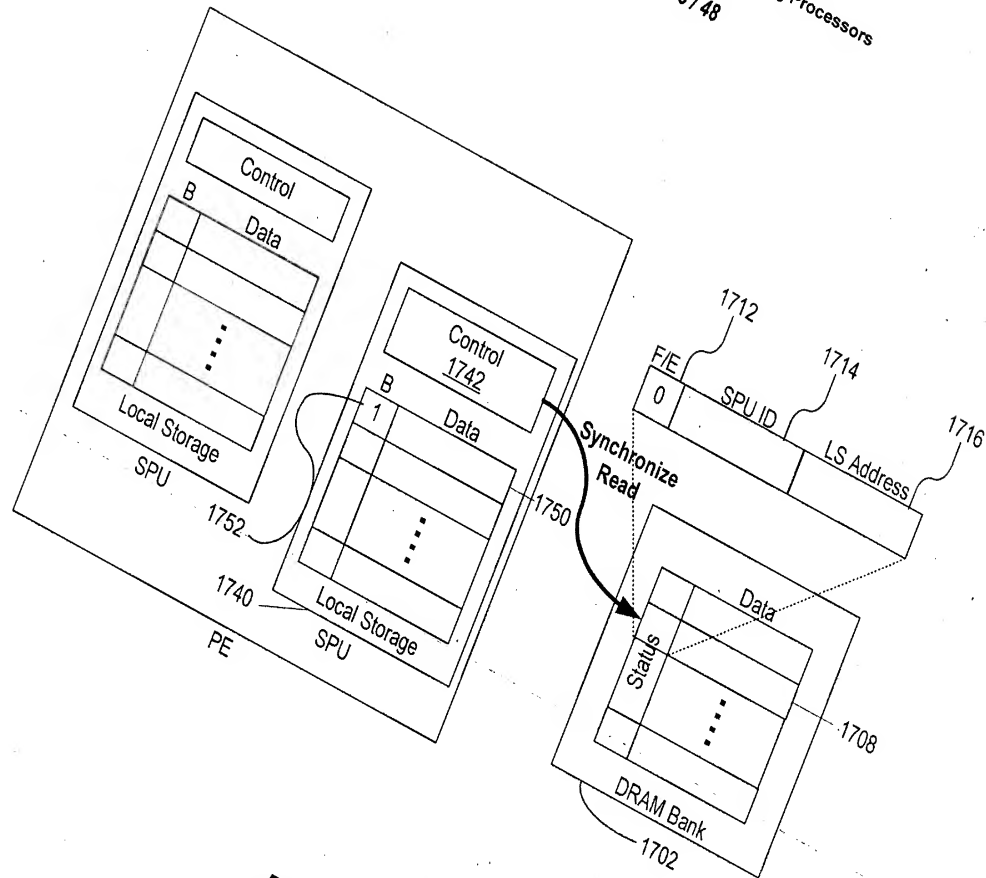


Figure 26

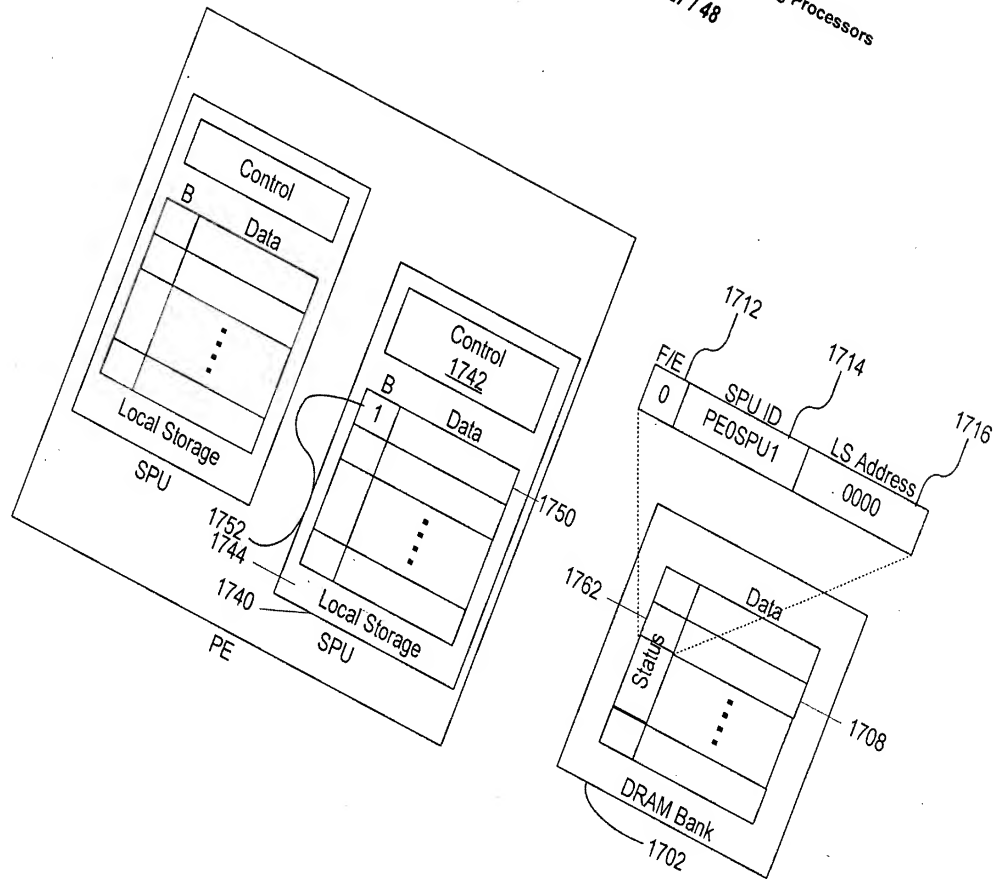


Figure 27

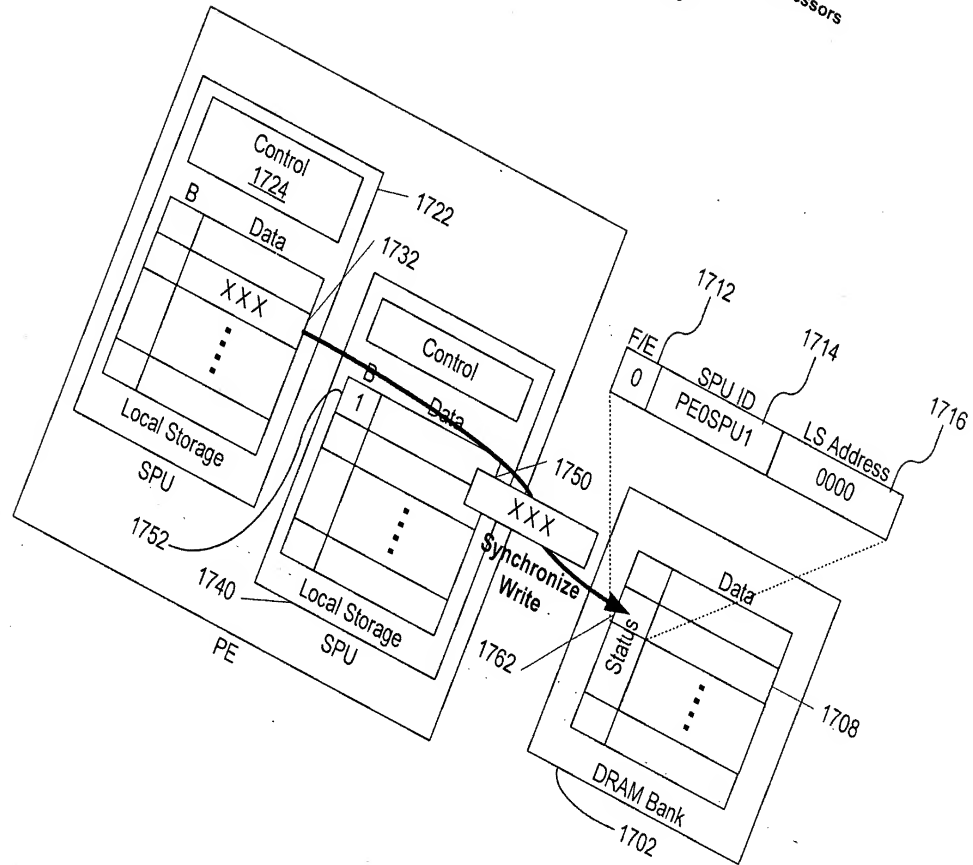


Figure 28

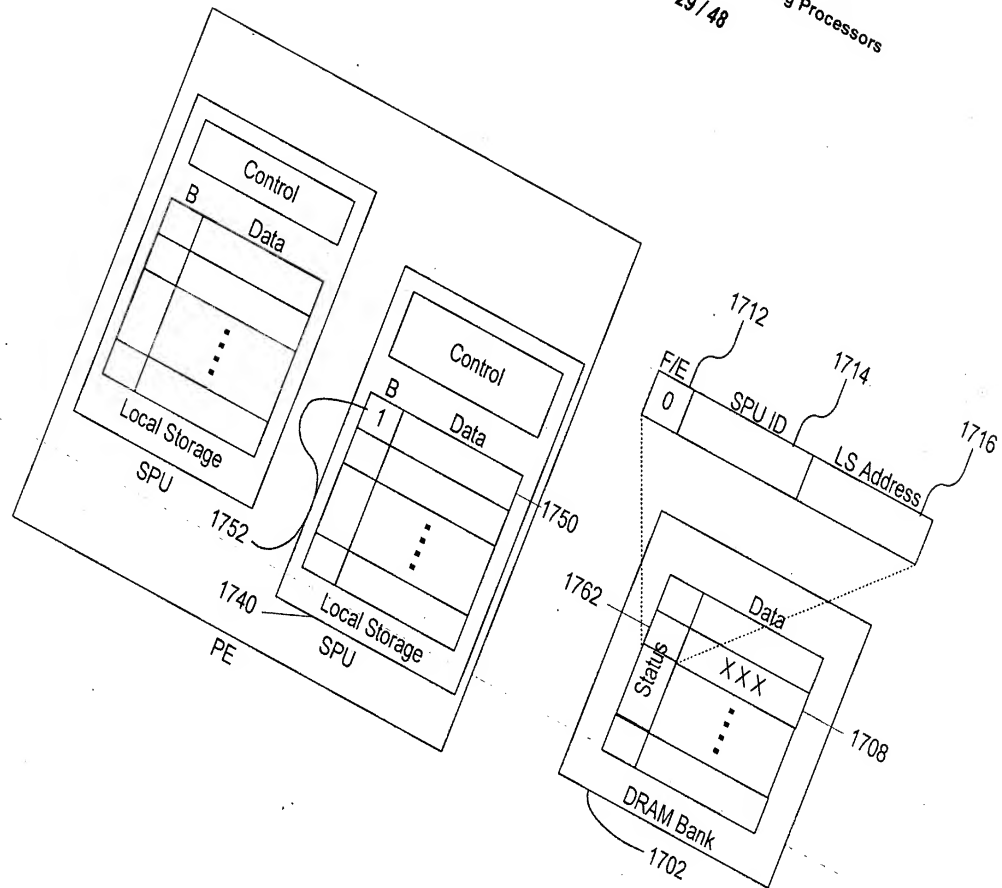


Figure 29

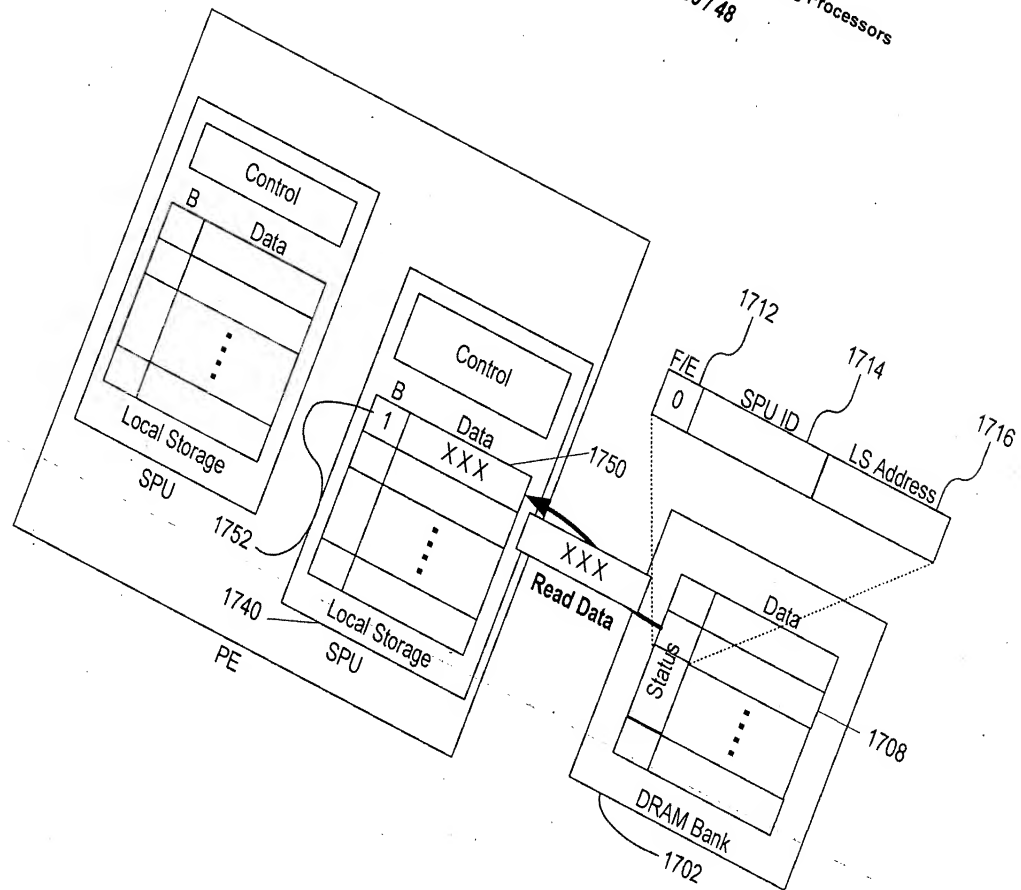


Figure 30

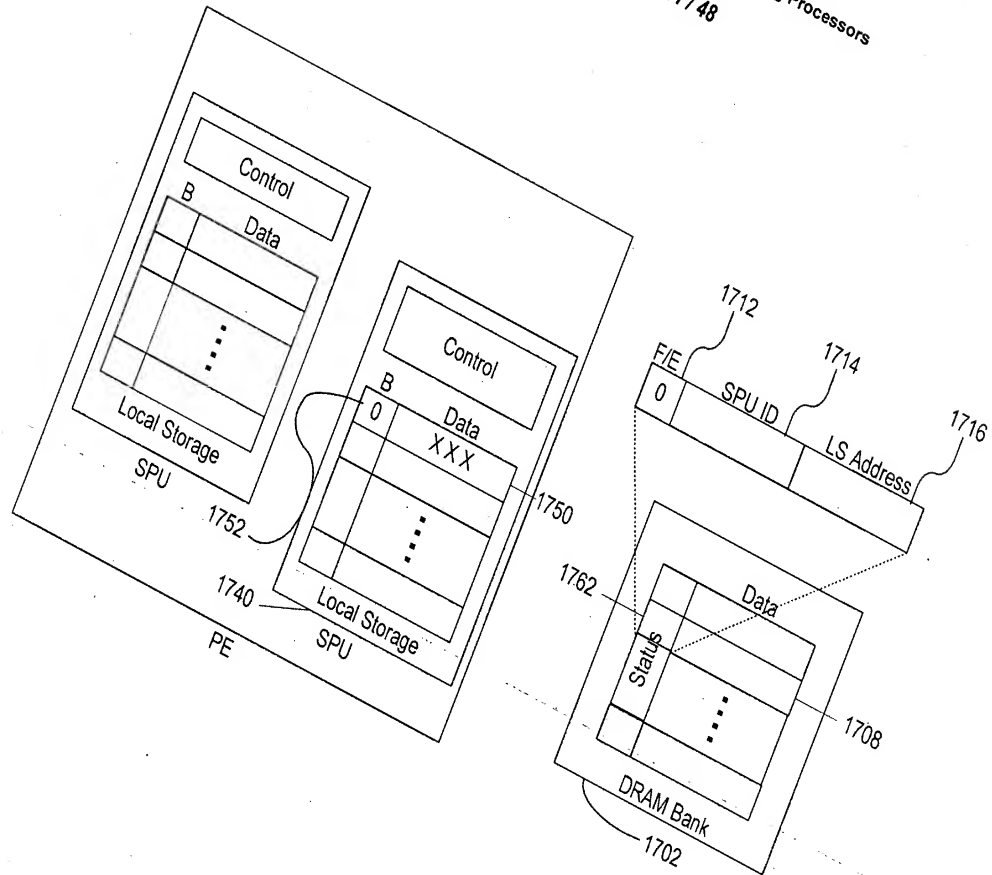
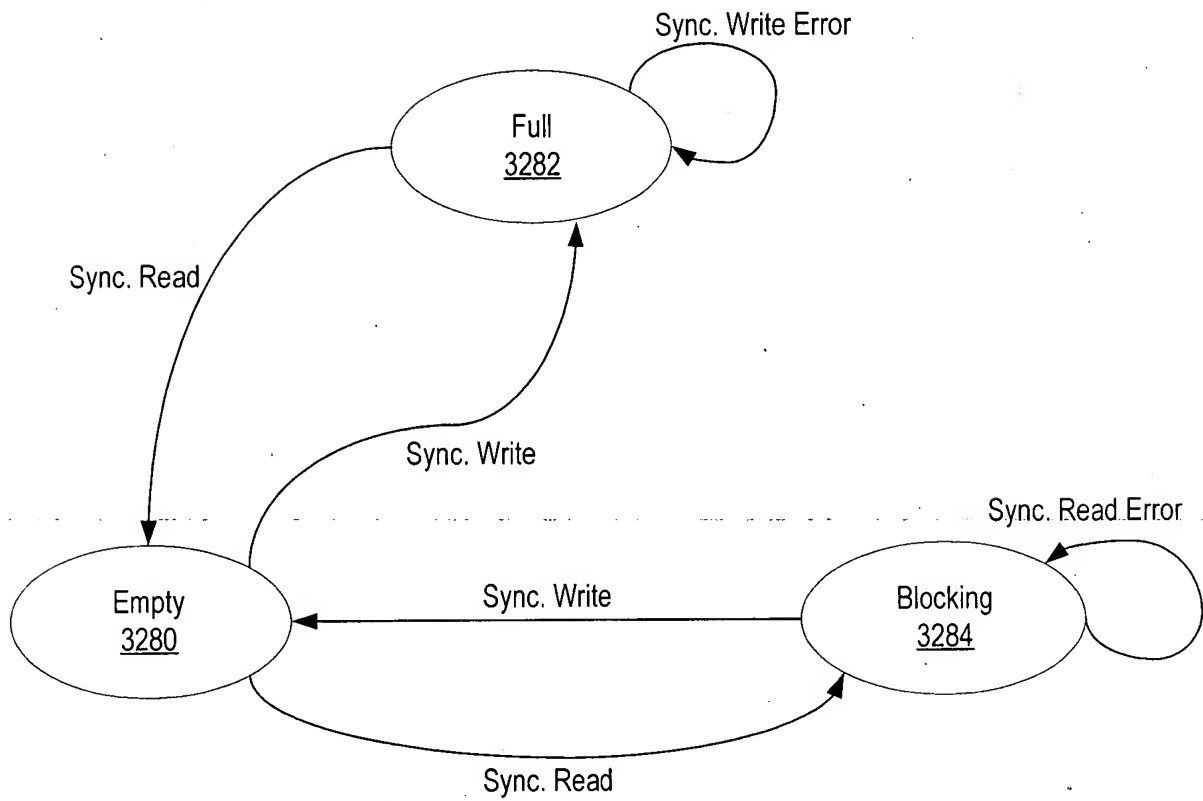


Figure 31

**Figure 32**

Key Control Table

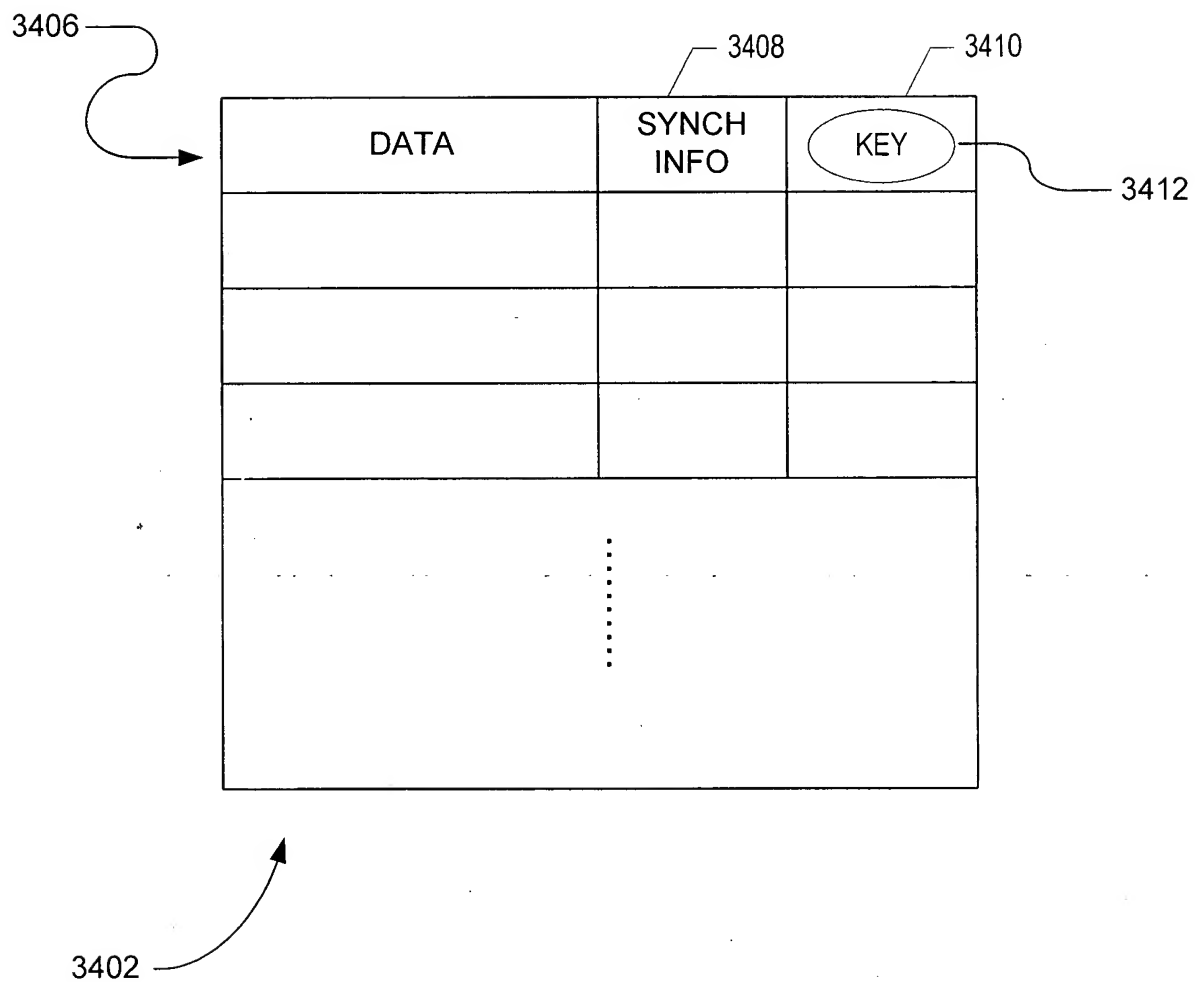
3302

3304 ID 3306 3308

0	SPU Key	Key Mask
1	SPU Key	Key Mask
2	SPU Key	Key Mask
		⋮
7	SPU Key	Key Mask

Figure 33

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**Figure 34**

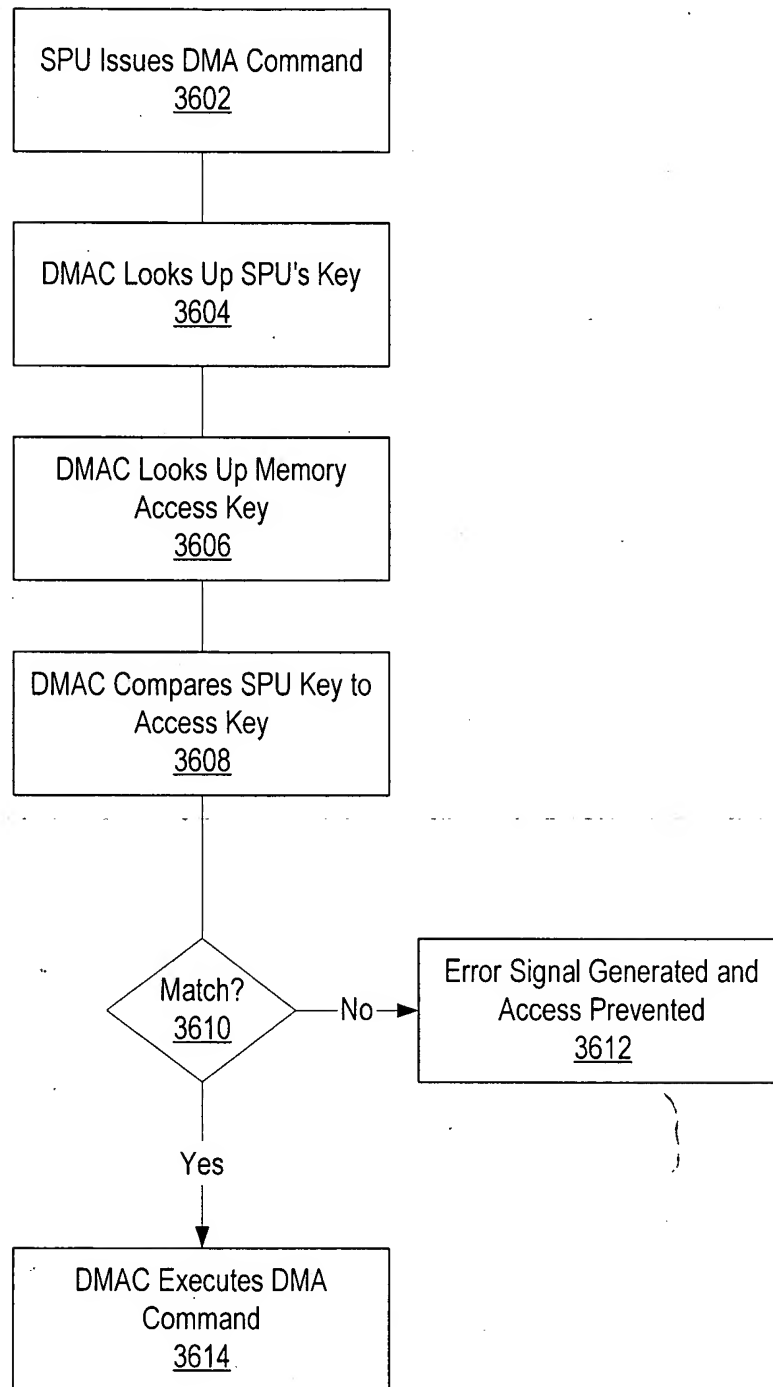
Memory Access Control Table

3504	ID	3506		3508	3510	3512
		0	Base	Size	Access Key	Access Key Mask
		1	Base	Size	Access Key	Access Key Mask
		2	Base	Size	Access Key	Access Key Mask
		...				
		63	Base	Size	Access Key	Access Key Mask

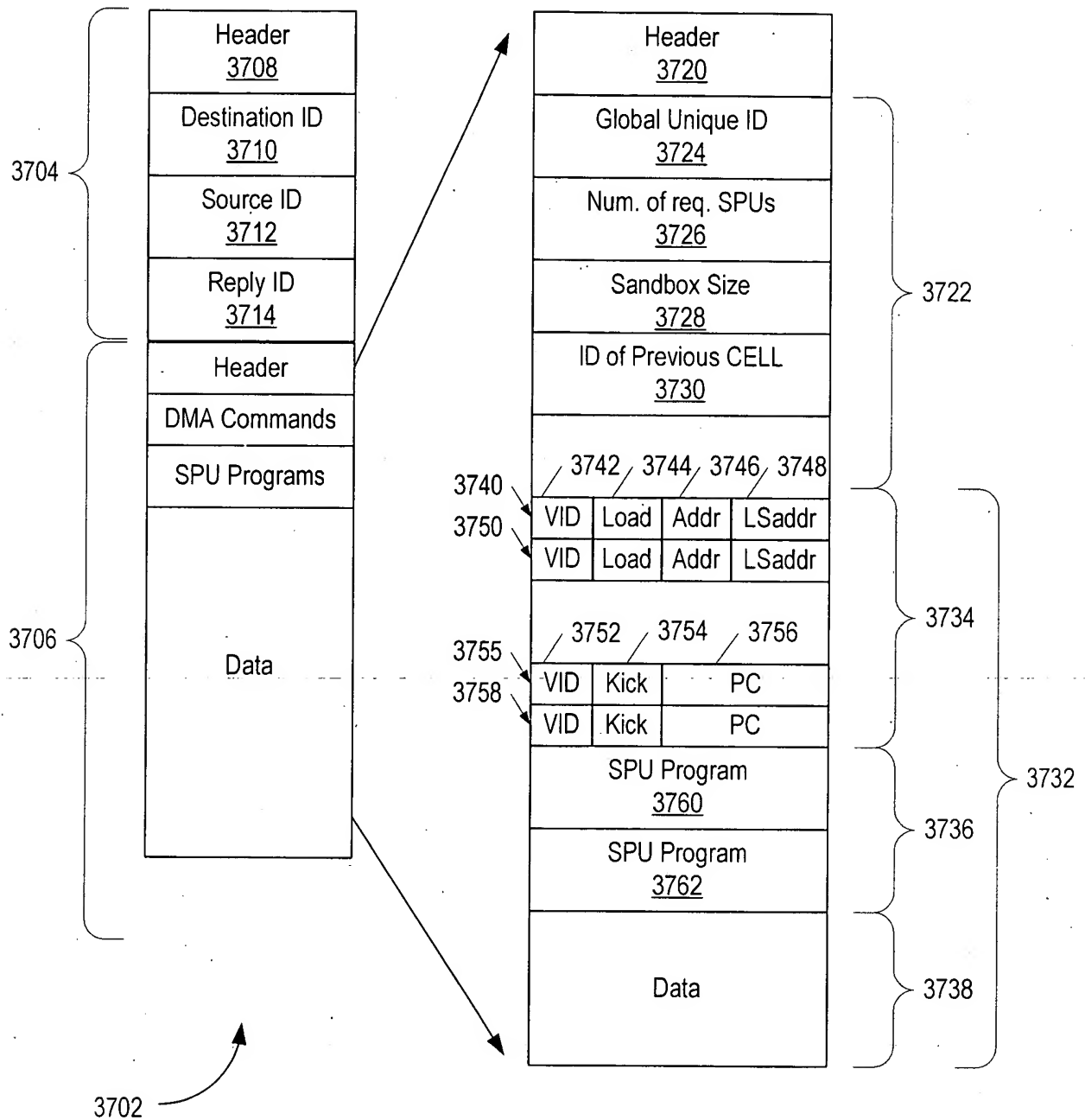
3502

Figure 35

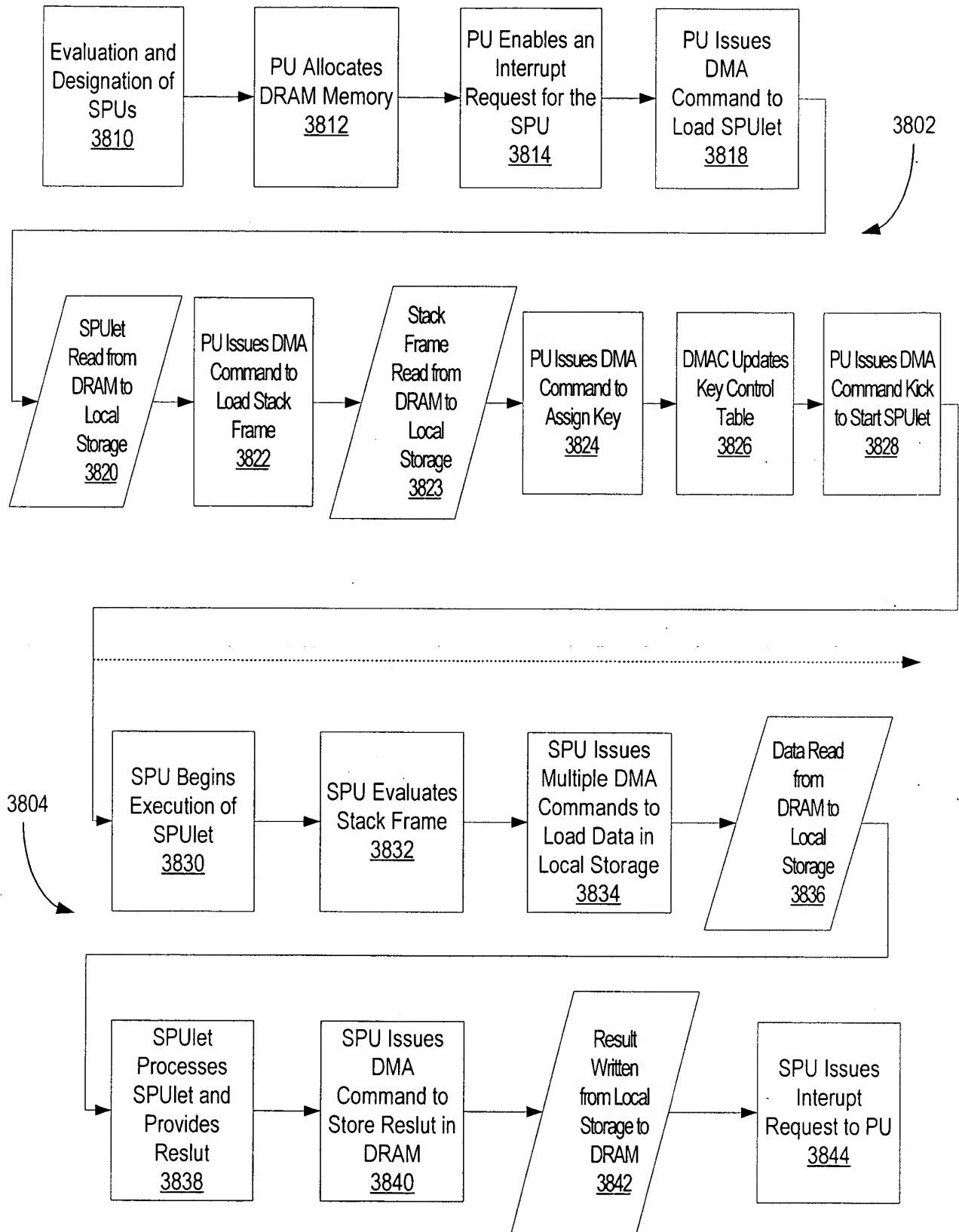
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**Figure 36**

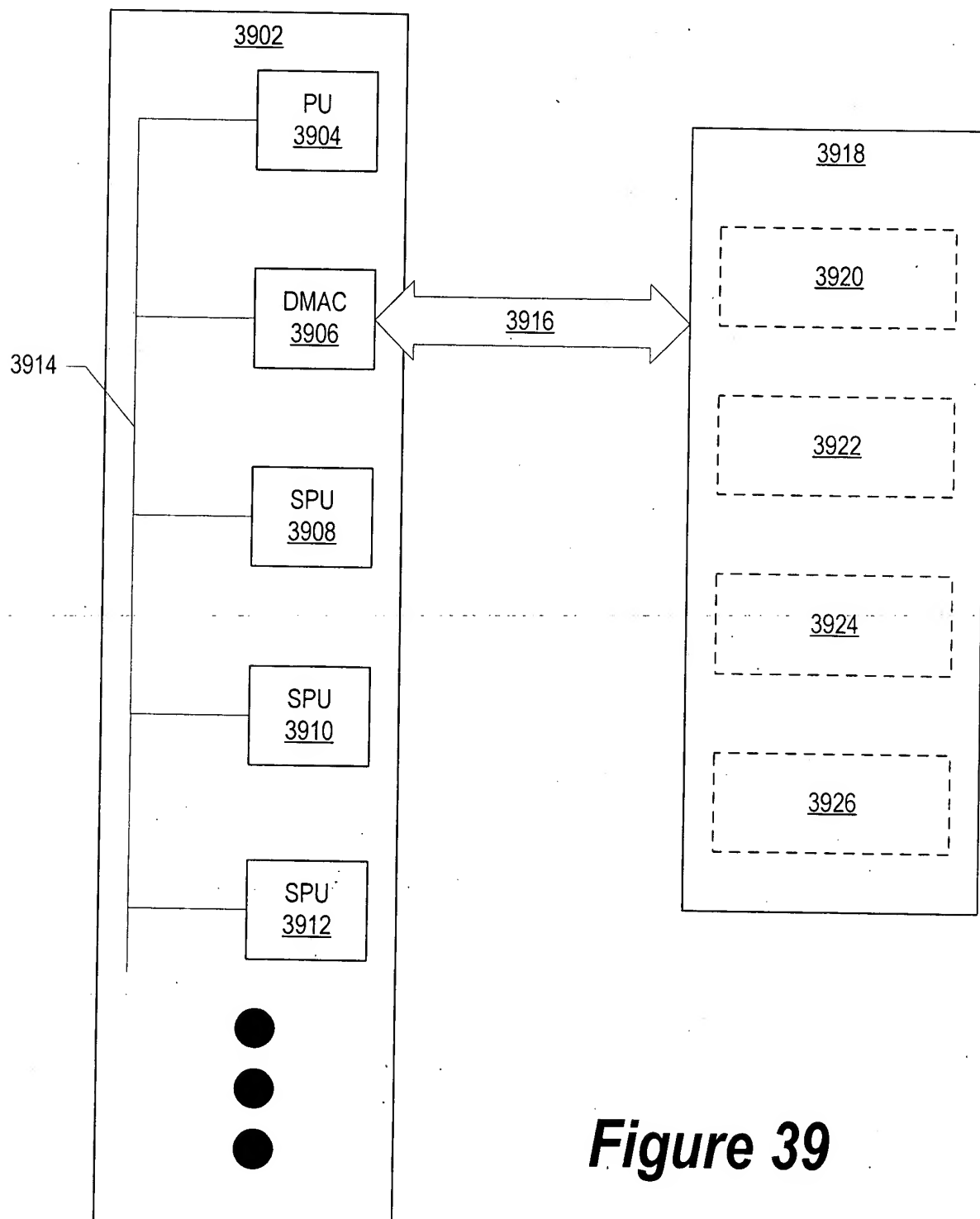
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**Figure 37**

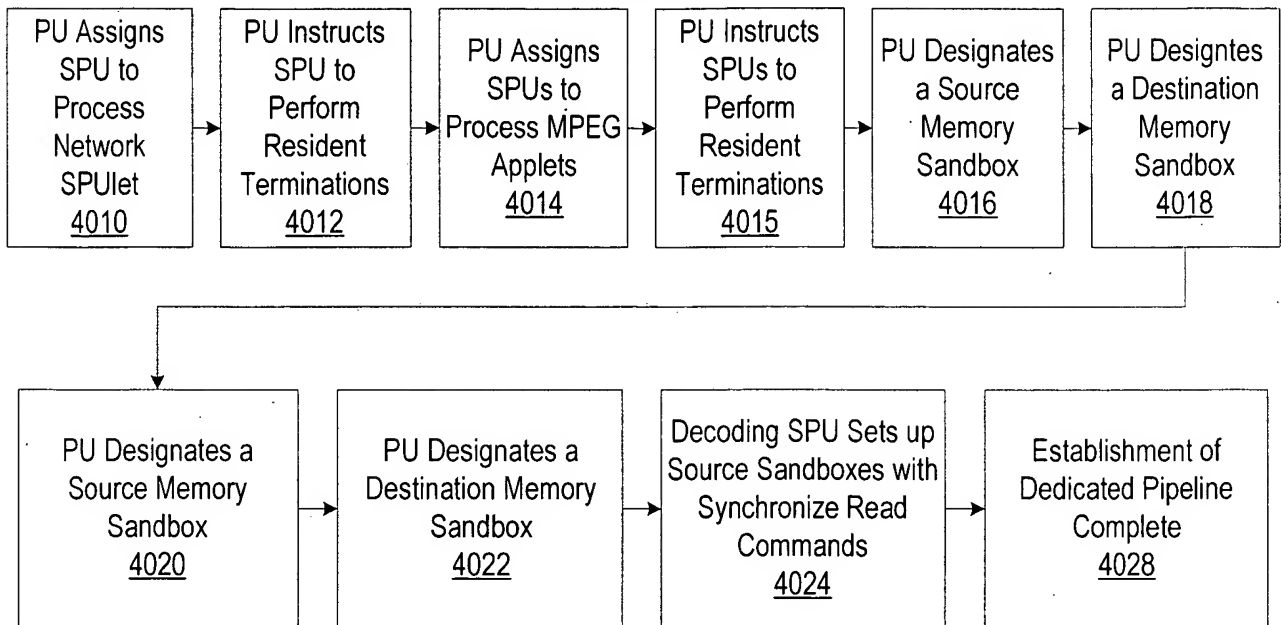
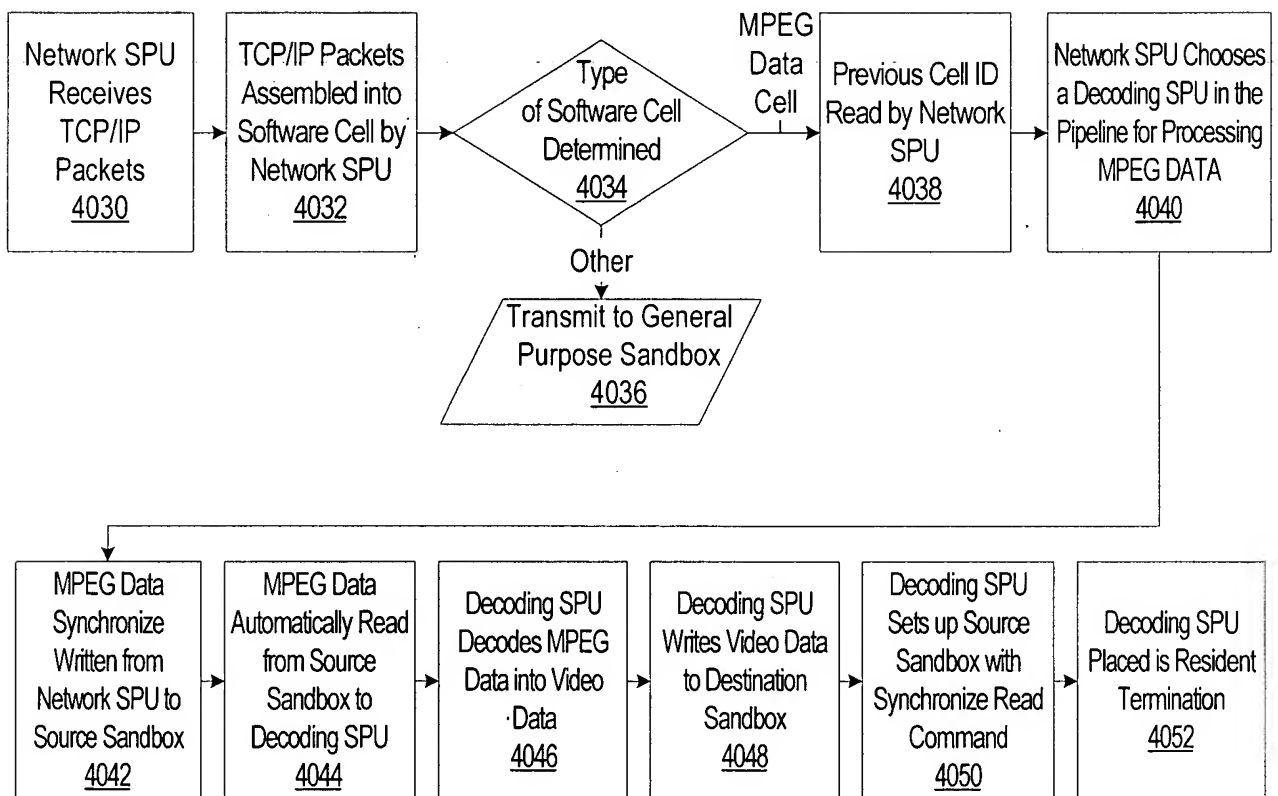
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**Figure 38**

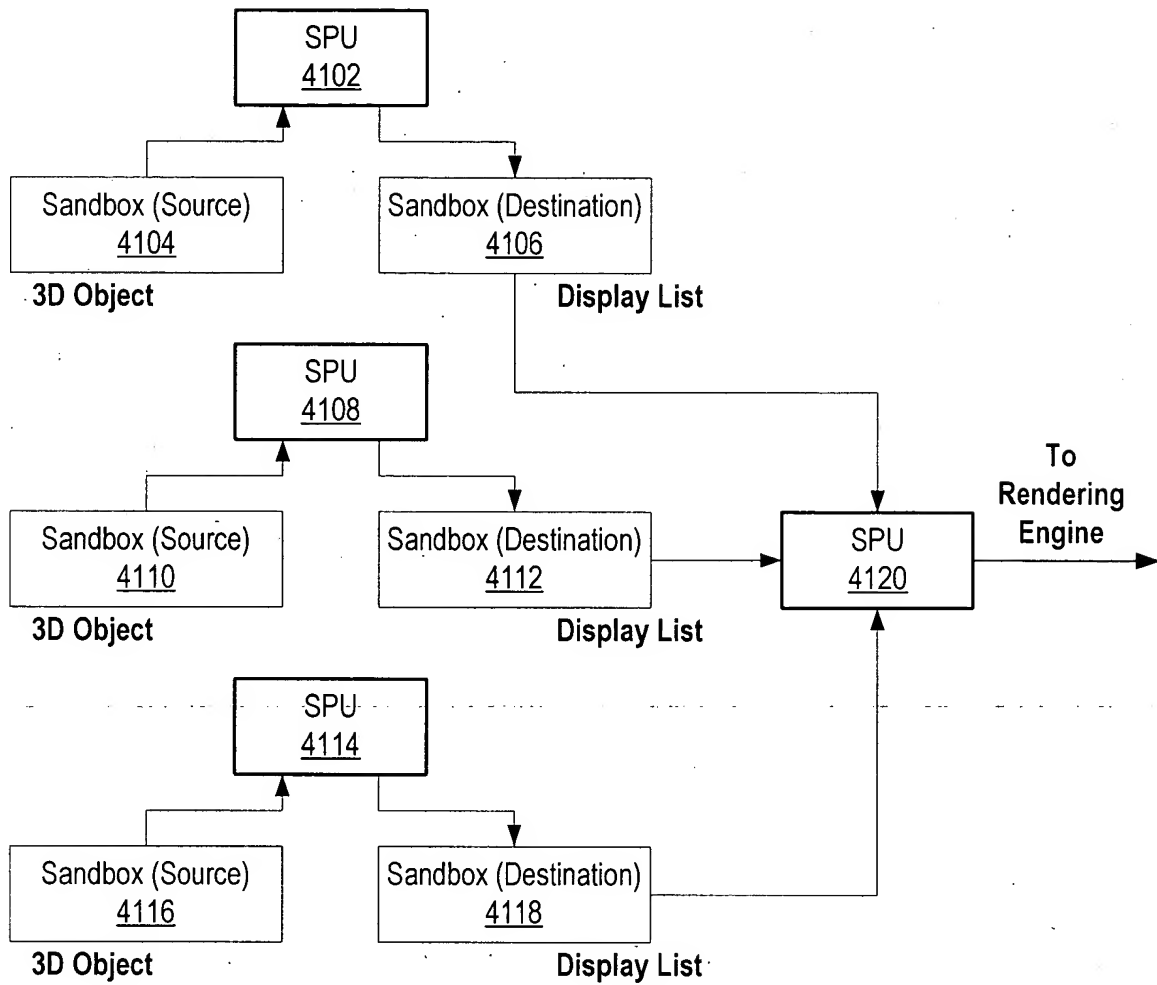
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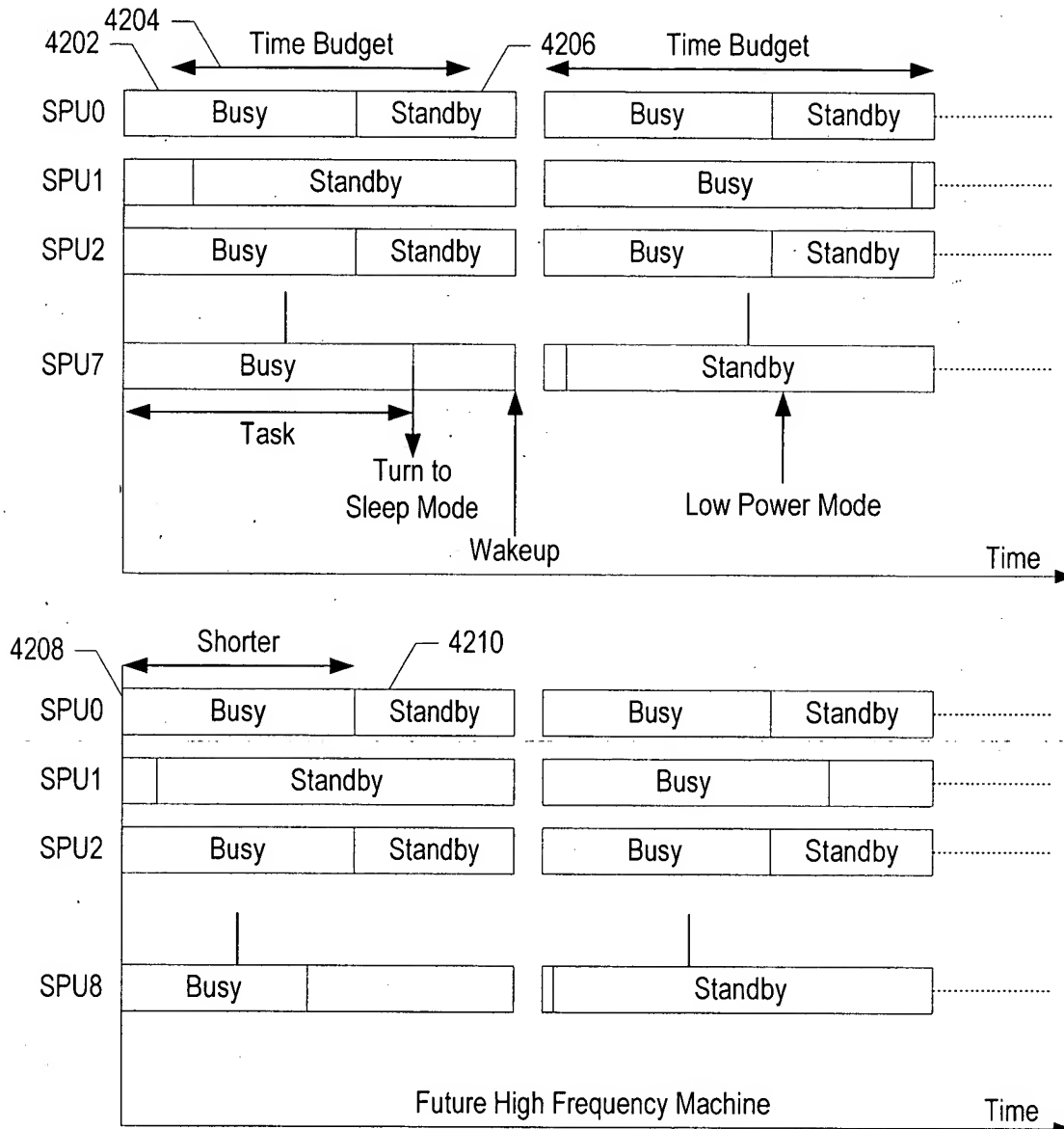
**Figure 39**

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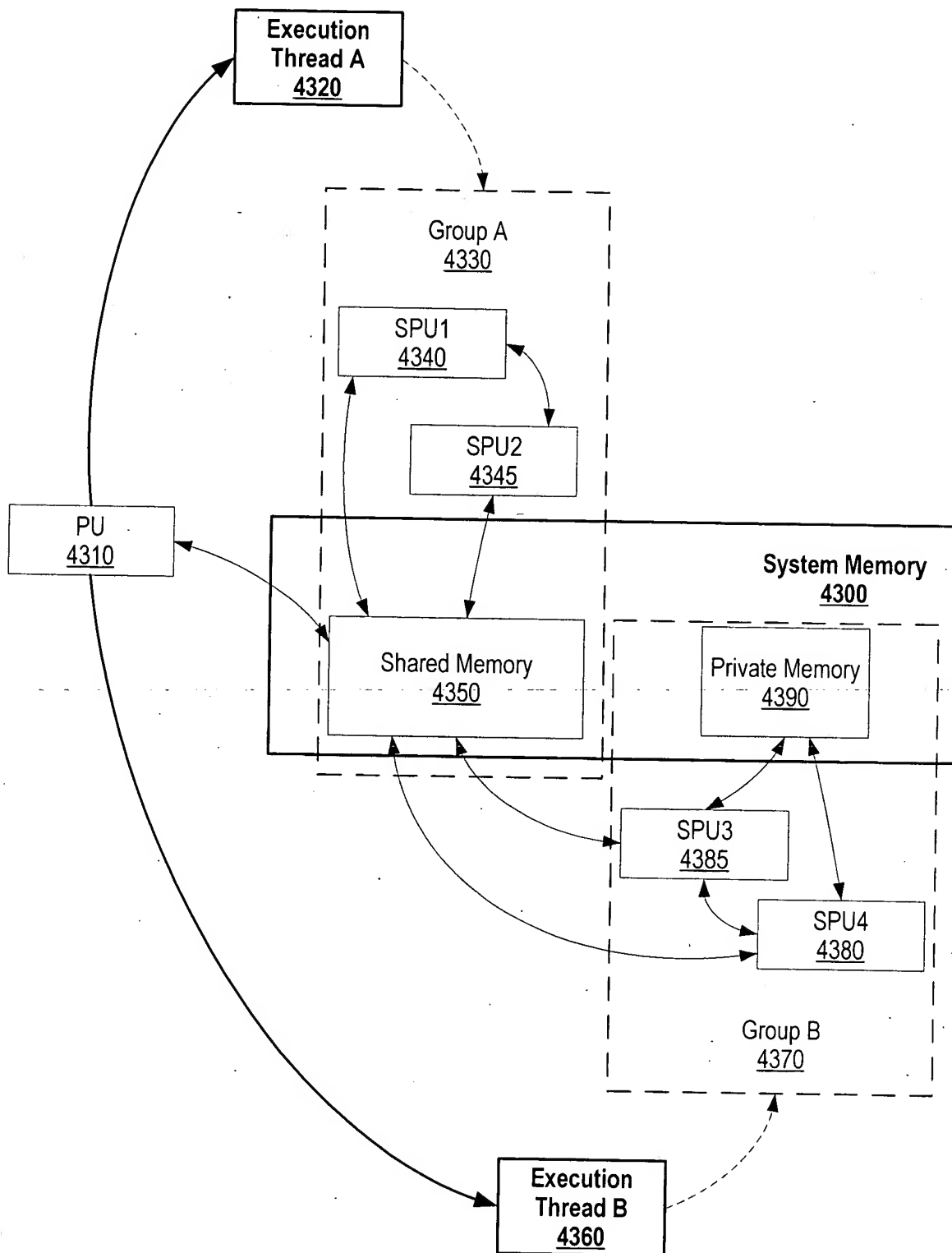
**Figure 40A****Figure 40B**

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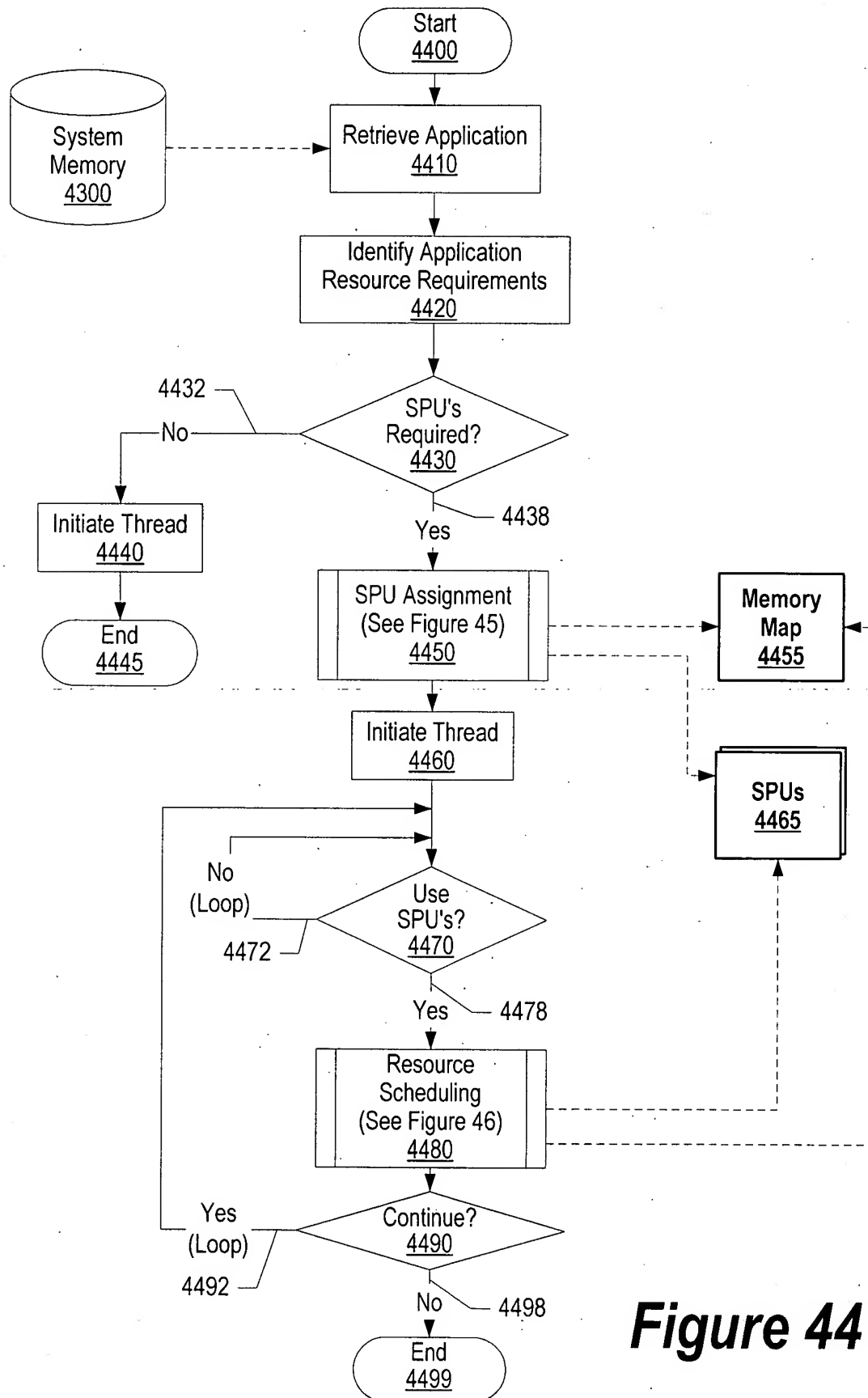
**Figure 41**

**Figure 42**

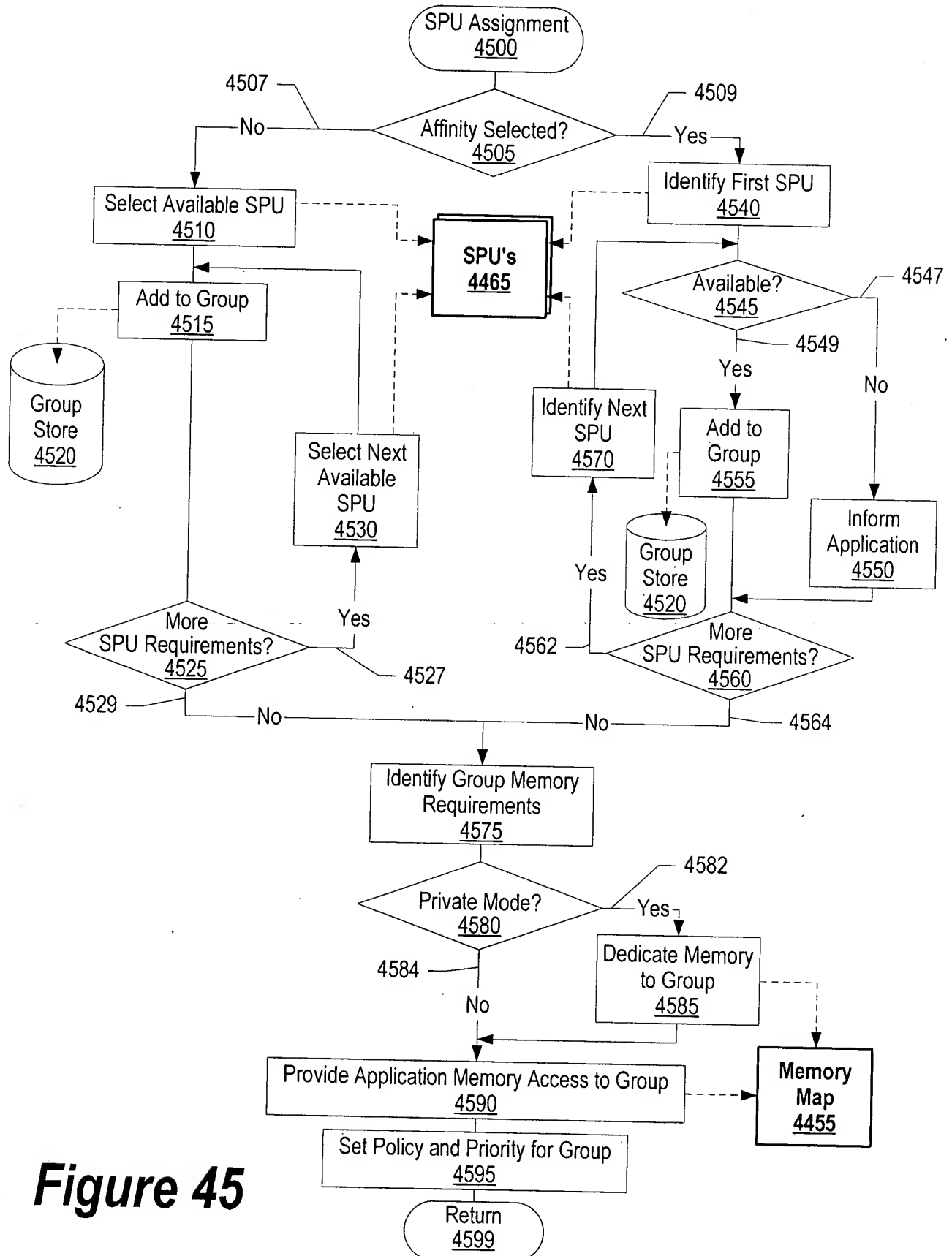
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**Figure 43**

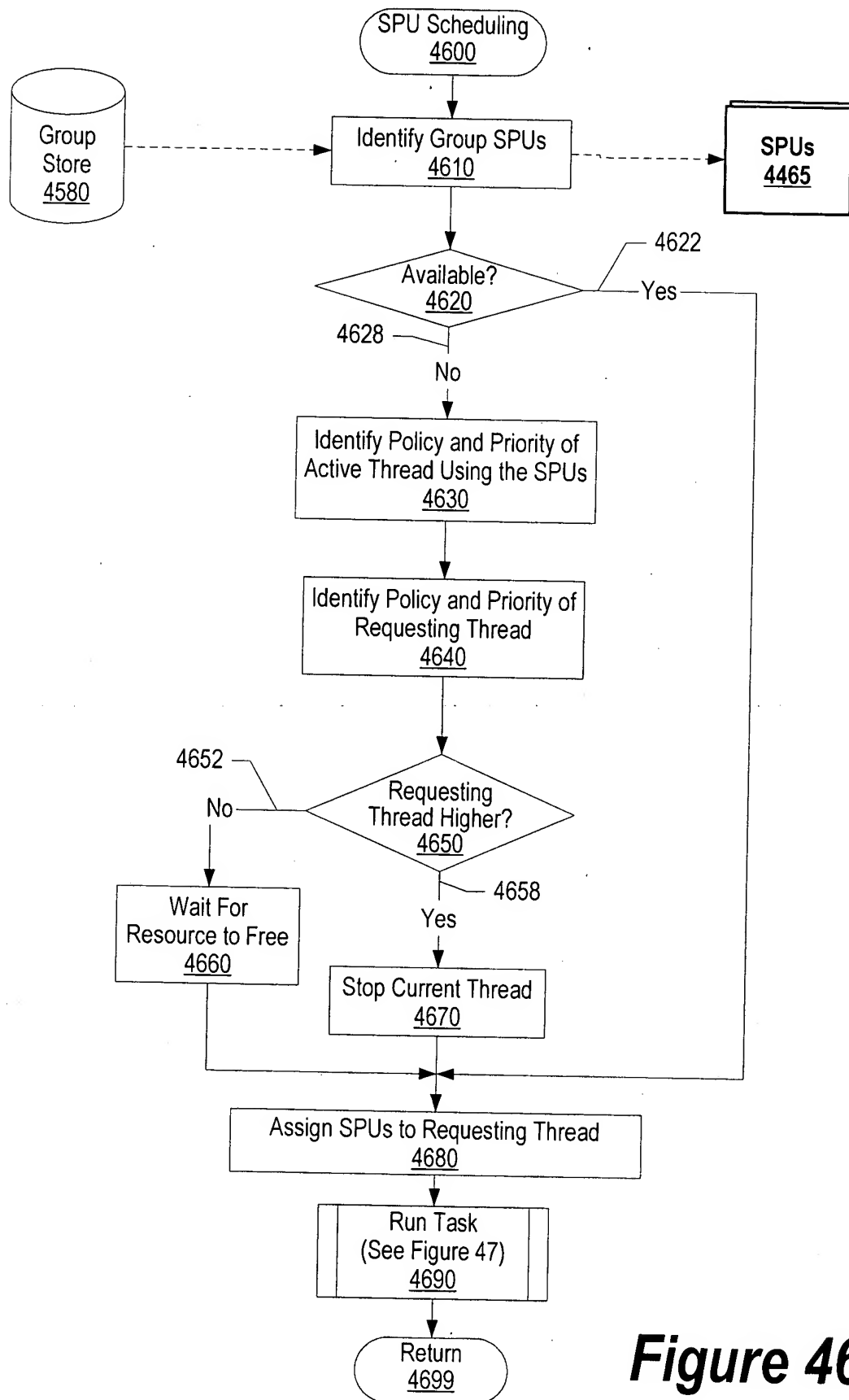
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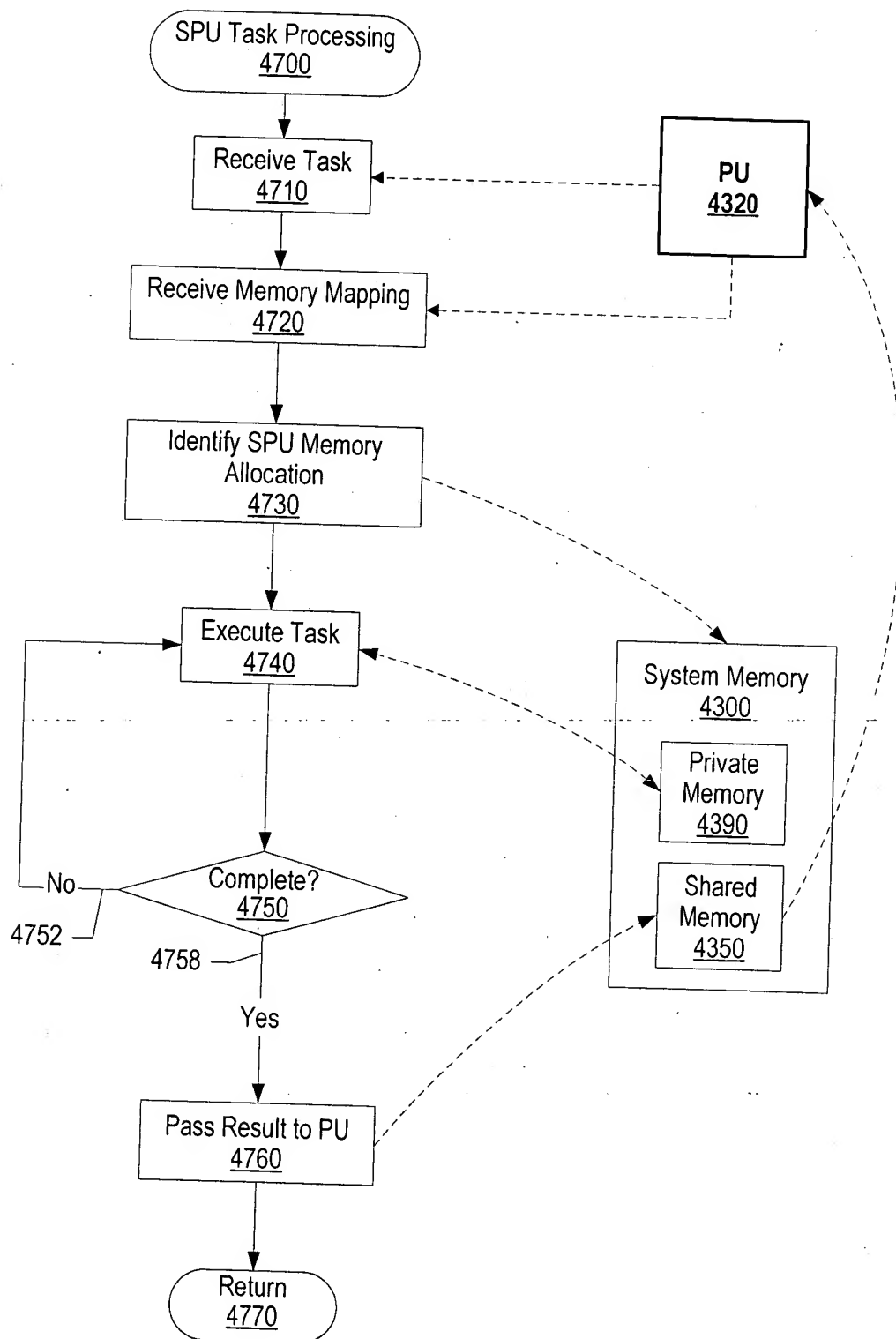
**Figure 44**

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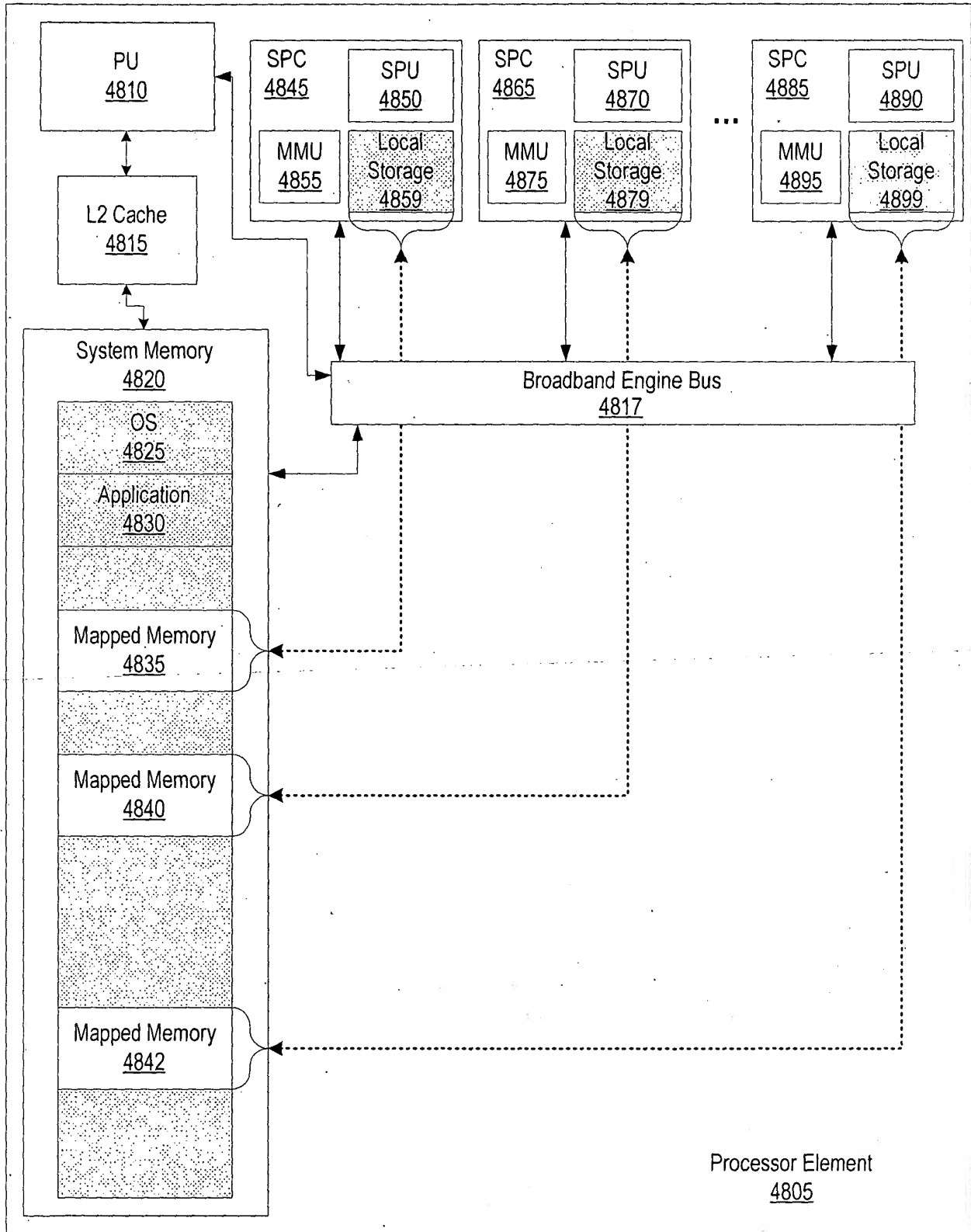
**Figure 45**

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**Figure 46**

**Figure 47**

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Processor Element
4805**Figure 48**